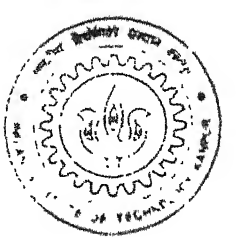
ACTIVE HARMONIC CURRENT COMPENSATION USING HARD AND SOFT-SWITCHED INVERTERS

by

KAMALAKANTA MAHAPATRA



DEPARTMENT OF ELECTRICAL ENGINEERING

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ACTIVE HARMONIC CURRENT COMPENSATION USING HARD AND SOFT-SWITCHED INVERTERS

A Thesis Submitted
in Partial Fulfilment of the Requirements
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DOCTOR OF PHILOSOPHY

by

KAMALAKANTA MAHAPATRA

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

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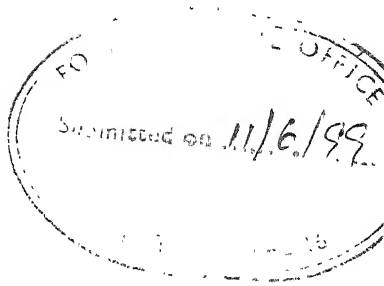

CERTIFICATE

This is to certify that the work contained in the thesis entitled " Active Harmonic Current Compensation using Hard and Soft-Switched Inverters" by Kamalakanta Mahapatra has been carried out under our supervision and this work has not been submitted elsewhere for a degree.

Arindam Ghosh

on leave
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Dedicated to

my family

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SYNOPSIS

The extensive use of non-linear loads results in harmonic pollution in a power distribution system. This leads to waveform degradation in power supply networks. A number of techniques such as use of passive filtering, active filtering, hybrid filtering etc. have been suggested in the literature for compensation of line current harmonics. However, all these schemes suffer from one or more drawbacks such as load dependence, large system size, inadequate current regulator bandwidth, poor system efficiency and complexity of control.

Passive filters that are made up of inductive and capacitive elements tuned to the harmonics to be compensated are used for compensating harmonics. These filters have certain disadvantages that are well documented in the literature. Active filters are currently regarded as the most efficient option to solve the problems created by non-linear loads [1].

The parallel active filter is the most common configuration for active filtering application. The filter is connected in parallel with the load being compensated. For the power circuit, an inverter operating in current control mode is used. The current

compensation is usually done in time domain for faster response. The purpose is to inject a compensating current at the shunt point such that the source current becomes sinusoidal. Since this compensator is used for canceling the harmonics we refer it as an *active harmonic current compensator (AHCC).* The reference current that the compensator must follow or track is a function of the load current. However, the load current is not known a priori. Moreover, the load may also change. Therefore a suitable strategy must be employed for the extraction of the reference current. This is one of the biggest challenges in an AHCC design.

Out of the several schemes suggested in literature, the hard-switched PWM inverter based shunt compensator has gained prominence. However, this compensator has its inherent limitations of high switching losses because of hard switching. Switching losses are one of the main restrictions that is put on the high operating frequency. It also requires a large dc link filter and hence its time response is sluggish. For proper current tracking, the approximate current bandwidth is usually the PWM frequency divided by a factor of ten. Therefore, PWM based compensator fails to track high frequency components, particularly at high power level. For example, if the harmonics up to nineteenth are to be cancelled for a 500 kilowatt converter load, then the compensator should have a power rating of 100 kVA and it must be capable of switching at a frequency of about 9.5 kHz or higher. This is a difficult task given the current state of the art of power semiconductor device technology. Using conventional switching techniques, inverters of over 10 kW are restricted to operate at frequencies of below 10 kHz. Without adequate current regulator bandwidth, compensation can never be perfect.

For active harmonic current compensation, a high power topology with adequate current regulator bandwidth is necessary. In essence, it is required to realize a large capacity non-sinusoidal current source generator, which must follow its command instantaneously.

An important inverter topology is the so-called resonant dc link inverter (RDCLI) [2]. This soft-switched inverter would provide adequate current regulator bandwidth because of its high frequency of operation, and hence an ideal candidate for active filtering application. Moreover, as the switches in this inverter are switched at zero voltage crossings (ZVS), the switching losses will be a minimum and hence the AHCC can achieve high efficiency. This simple topology however has few drawbacks. These

are higher device voltage stresses (when the output voltage is greater than twice the dc input voltage), zero crossing failure unless the initial current in the resonant inductor is built properly.

Keeping in view of the above considerations we define the following objectives of the thesis.

1. To find out a suitable topology for AHCC such that the compensator would achieve high efficiency, provide adequate current regulator bandwidth and fast transient response
2. To devise a suitable control strategy for the extraction of compensator current reference.
3. To study the different control aspects of the AHCC such as current regulation within the inverter and any other control required for the inverter.
4. To evaluate the performance of the AHCC in terms of compensation, response time, efficiency etc. through simulations and experiments.

The major contributions of this thesis are:

1. A suitable topology for the power circuit of AHCC application is determined. Different power converter topologies are investigated for active filtering application. It is possible to achieve compensation with a hard-switched PWM inverter based compensator when its switching frequency is high. However, the increase in frequency will result in increased losses and higher device stresses. On the other hand a soft-switched inverter based AHCC is able to compensate all load harmonics because of high frequency switching. Furthermore, this compensator is efficient in the sense that the switching losses are a minimum.

   It is demonstrated that a three-phase AHCC would work provided the dc side capacitor is split into half and the neutral is connected to the load neutral. A topology for three-phase AHCC is proposed, in which three single-phase RDCLI energized by a single dc capacitor is used as the power circuit. These inverters are connected to the ac bus through three different isolation transformers.

2. In this thesis a new current initialization scheme is proposed for a resonant dc link inverter (RDCLI) [3]. The method of current initialization is based on the state transition analysis of the system as a boundary value problem (BVP). It is shown

that for a given load current, it is possible force the dc link voltage to go to zero at a prescribed time by properly choosing the initial dc link current. This technique makes it possible to operate the resonant dc link inverter without any zero-crossing failure, which is an important issue for a satisfactory operation of such an inverter.

3. In this thesis two methods are proposed for the extraction of active fundamental current of the load current. In the first method, the error in the dc capacitor charge is passed through a controller. The output of this controller is multiplied by the template of the source voltage to give the desired source current. The reference for the compensator is obtained by subtracting this value from the instantaneous value of load current.

   In the second method the average value of the capacitor current over one cycle is passed through a controller to give the loss component of the AHCC. This quantity is added with the peak value of the source current (obtained through power calculation) and is then multiplied by the template of source voltage. The resultant quantity gives the instantaneous value of the desired source current. The reference current for the compensator is obtained by subtracting the desired source current value from the instantaneous value of load current. It is possible to extract the compensator reference using the above two methods. However, the response of the second controller is slow when compared to the first one.

4. For the proposed charge based model two controllers are investigated [4]. The PD controller gives a superior performance compared to the PI controller. The PD controller has a faster response, better stability margins. The AHCC losses decrease with a PD controller to a certain extent.

5. PC interface is used for the implementation of the proposed current initialization scheme. The use of a PC makes the system more flexible for conducting experiments. This facilitates zero-voltage switching by taking into account of the actual circuit delays and tolerances.

OUTLINE OF THE THESIS

Chapter 1 introduces the concept of active filtering. The basis for this problem along with literature review is presented. The objective of the thesis and outline of the thesis is also presented.

Chapter 2 begins with a discussion on multilevel inverter and more specifically on a three-level inverter. We then discuss a three-level inverter based active harmonic current compensator. A closed-loop model in conjunction with PD controller is proposed for extraction of compensator reference. The performance of this compensator in conjunction with the PD controller is evaluated. The compensator is able to compensate load harmonics and has a fast transient response. However, in the presence of unbalance in the load, the circuit response becomes slow. All the above points are demonstrated through digital simulation.

In Chapter 3 we demonstrate the use of a soft-switched RDCLI as an AHCC. A new current initialization scheme is proposed that ensures ZVS. The performance of this topology as an AHCC is investigated. The current control in the inverter is done through zero-hysteresis bang-bang control. The inverter switching state selection is done to achieve regulation objectives. This compensator performs reliably for balanced load conditions. However, its performance degrades under unbalanced load conditions because of the unconnected neutral. These points are highlighted in this chapter.

In Chapter 4 single-phase hard-switched inverter based AHCC is considered. Two control strategies are discussed for extracting the compensator reference. As shown through digital simulation, the performance of the compensator is quite good.

In Chapter 5 we consider two different soft-switched inverter topologies that can be used single-phase AHCC. First the performance of the RDCLI based on the current initialization technique described in Chapter 3 is investigated, vis-a-vis its switching frequency and dc voltage level. Next we consider a quasi-resonant dc link inverter (QRDCLI) based AHCC. It is shown that a QRDCLI based AHCC, even though more complex than an RDCLI based AHCC, does not have an improved performance over the RDCLI based AHCC. All these are demonstrated through simulation studies. Further a topology for three-phase AHCC is also proposed in which three single-phase RDCLI that are driven from a single dc storage capacitor is used as power circuit.

Simulation results show that this topology offers much improved performance than a three-phase RDCLI based AHCC.

In Chapter 6 experimental setup for the single-phase RDCLI based AHCC and PWM inverter based AHCC is described. Details of the power circuits, various control circuits and PC interface are presented. The use of PC for the current initialization makes the circuit simpler and flexible.

In Chapter 7 we present the experimental results obtained in the laboratory through lab prototypes. For purpose of comparison, some further simulation results for load cases identical to those in experimental setup are also obtained. The experimental results are in close agreement with the theoretical results obtained in the earlier chapters thus validating the concepts presented in this thesis.

In Chapter 8 the general conclusions derived from this thesis are presented. This chapter also presents some future directions for research in the area of AHCC.

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CHAPTER 1

INTRODUCTION

Currently there is a growing concern regarding power distribution system harmonic currents and power quality. The increasing use of power electronic based loads is increasing harmonic distortion levels in end use facilities and on the overall power system. Today many utilization equipment are being designed and built using power-electronic based power supplies, more specifically switch-mode power supplies (SMPS). Microwave ovens, laser printers, medical instrumentation, stereos, televisions and electronic lighting are few examples that use switch-mode power supplies. Other types of nonlinear loads include light dimmers, 6-pulse rectified supplies, 6-pulse phase-angle controlled loads and 12-pulse rectified supplies. Variable speed drives are exhaustively used for motor drive applications. They use 6-pulse rectified and phase-angle controlled power supplies to improve efficiency and controllability of the drive system. Thus power-electronic loads are integral parts of modern appliances and industrial loads.

These power electronic based loads are essentially non-linear because of the way they draw power. Usually such loads draw a distorted, non-sinusoidal (non-linear) current waveform. These currents have a high harmonic content and may have a poor power factor. Some of the adverse effects of concentrated nonlinear loads upon a facility are:

- Voltage distortion
- Excessive neutral return currents
- High levels of neutral-to-ground voltage
- Overheated transformers
- Poor power factor

These are matters of serious concern both for customers and utility. On the other hand, the demand for clean power in the use of sensitive loads such as computers, medical electronic equipment and automated processes continues to grow. There have been efforts from various quarters to mitigate these load current harmonics that otherwise would be drawn from the supply. A number of techniques such as active filtering [1,2], use of passive filter [3], hybrid filtering [4] etc. have been suggested in the literature for harmonic cancellation.

Passive filters that are made up of inductive and capacitive elements tuned to the harmonics to be compensated are used for compensating harmonics. These filters are connected in parallel with a harmonic current generating load thus providing a short circuit path for the harmonic current. However, passive filters have certain disadvantages [3,5]. These are:

- The application of passive tuned filters creates new system resonances that are dependent on specific system conditions.
- Passive filters often need to be significantly overrated to account for possible harmonic absorption from the power system.
- Passive filter ratings must be coordinated with reactive power requirements of the loads.
- The number of passive filters installed must be equal to the number of harmonics to be compensated.

In addition to the above, the size and cost associated with passive filter have forced the development of new compensation techniques in the shape of active filters. Active filters are currently regarded as the most efficient option to solve the problems created by non-linear loads [1,6].

1.1 ACTIVE POWER FILTERS

An active filter uses power electronics to produce harmonic components that cancel the harmonic components of the non-linear load. This harmonic filter includes a power converter and a control loop, which controls the harmonic injection of the filter into the ac network based on the measured load harmonics. Therefore, this device senses voltage

and current harmonics and generates offsetting harmonics to cancel out the unwanted harmonics in the source. There obviously exists a feedback mechanism by virtue of which the source provides clean waveforms for the load. Voltage regulation and power factor control are also normal byproducts of this filter operation. Some of the benefits of using active filters are:

- Harmonic reduction
- Reduction of 3-phase neutral return current
- Impact minimization upon distribution transformers
- Power factor improvement
- Voltage regulation

There are many approaches adopted for active filtering [1,2], which are also termed as active power line conditioners in the literature. Depending on the structure and configuration, an active filter can either compensate the harmonic currents emitted by a non-linear load, or compensate, at the terminals of the load, the harmonic voltages that pre-exist in the distribution system network. Certain harmonic filter structures combine passive and active systems to achieve performance levels similar to those of an active filter [4]. Series active filters require low power PWM voltage source inverters to generate the harmonic voltage components necessary to isolate the respective current harmonics from the power source. These filters present excellent current harmonic compensation. Their main disadvantage is related with the protection scheme that has limited their application in power distribution system [1]. As a result, shunt active power filters have gained prominence among various active filtering topologies.

1.2 ACTIVE FILTER CLASSIFICATION

The voltage waveform at a system bus gets affected by the non-sinusoidal currents injected at that bus. Provided that the ac bus is stiff, the voltage at that point would not be affected because of non-linear current drawn. However, if an ac bus is not too stiff, the voltage at that point would be distorted the moment non-sinusoidal currents are drawn from the source. Now this voltage waveform must be corrected to sinusoidal by injecting the proper current at this point.

Active filter classification by objectives is done in [1]. Here objective means, "who is responsible for installing active filters". This includes active filters installed by individual consumers on their own premises and active filters installed by electric power utilities in substations and/or on distribution feeders.

Active filter classification can be done through different viewpoints [1,2]. They can be classified based on the converter topologies used, control strategies adopted, type of configuration used etc. These are briefly discussed below.

1.2.1 Shunt or Series

Shunt active filters is the most common configuration. It is connected in shunt (or parallel) with the load. This is controlled to draw (or supply) a compensating current from (or to) the utility so that it cancels the load harmonics. The series active filter is connected in series with the utility through a matching transformer. A Shunt compensator injects currents while a series compensator injects voltages. The problem of protection restricts the use of series active filters. We shall therefore concentrate only on shunt filters.

1.2.2 Inverter Topology

Active filters can also be classified by the type of inverter topologies used. Two types of power circuits are usually used for active filters. These are voltage source inverter [7] or a current source inverter [8]. To be used as shunt active filters, both these must inject current into the ac system.

1.2.3 Time or Frequency Domain Correction

The reference current for the active filter can be generated either in frequency domain [9, 10] or in the time domain. For both these cases the power circuit can be a voltage source inverters (VSI) or a current source inverters (CSI). In the frequency domain correction, fast Fourier transform (FFT) is performed on the sampled load current waveform. Then a current waveform is reproduced that has same harmonic components with the opposite phase angles. However, this method would require a digital signal processor (DSP) platform to perform FFT calculations. Basically this calculation is performed in each cycle and the desired compensation is implemented in the successive

cycles. Therefore this clearly introduces one cycle delay and could be a problem for non-linear loads with rapidly varying characteristics. On the other hand in time domain compensation the instantaneous compensator current is obtained through sensing voltage and/or current signals and performing computations online.

1.2.4 The Approach used in this Thesis

In this thesis we have chosen the parallel or shunt configuration, i.e., the filter is connected in parallel with the load being compensated. For the power circuit, we employ a VSI operating in current control mode. The current compensation is done in time domain for faster response. The purpose is to inject a compensating current at the shunt point such that the source current becomes sinusoidal. Since this compensator is used for canceling the harmonics we term it as an *active harmonic current compensator (AHCC)*. Sometimes we shall refer it as compensator.

Fig. 1.1 shows the schematic diagram of an AHCC. The dc side of the AHCC is connected to an energy storing capacitor and the ac side of the inverter is connected to ac bus through a filter inductor (also called an interface inductor). The point (p) at which the AHCC is connected to the power system is called the point of common coupling. The ac bus can supply various loads including the non-linear ones. The compensator is controlled in a closed-loop manner — the inverter switches are controlled to actively shape the current through the interface inductor (i_F in Fig. 1.1) following a command current such that the input current from the source (i_S in Fig. 1.1) is in phase and of the same shape as the input sinusoidal voltage. The compensator supplies reactive and harmonic components of the load current and hence the source will be required to supply only the in-phase fundamental component of the load current.

The current waveform for canceling harmonics is achieved with the voltage source inverter and an interfacing inductor. This interfacing inductor or filter provides large isolation inductance to convert the voltage signal created by the inverter to a current signal for canceling harmonics. The desired compensator (injected) current waveform is obtained by accurately controlling the switches in the inverter. Control of current waveshape is limited by the switching frequency of the inverter and by the available voltage across the interfacing inductance. The voltage across the interfacing inductance

determines the maximum di/dt that can be achieved by the compensator. This is important in the sense that relatively high values of di/dt may be needed to cancel higher order harmonic components. Therefore the choice of the size of the inductor is crucial. A large inductor would be better for isolation from the power system and protection from transient disturbances. However, at the same time the large inductor would limit the ability of the compensator to cancel higher order harmonics.

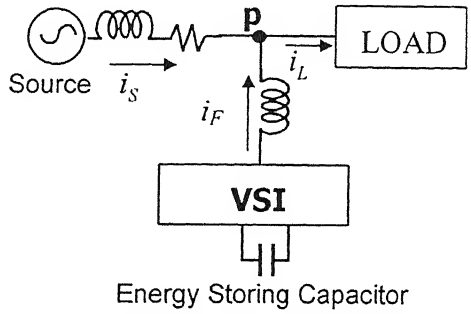


Fig.1.1 Schematic diagram of an AHCC

For this configuration, it is important to know the current the compensator is required to supply. In an ideal situation, the compensator is required only to supply the reactive power of the load and hence the average dc capacitor voltage should remain constant. In practice, this however is not true as the losses of the inverter and interface inductor will make the dc charge stored in the capacitor to fall. However, it is important to keep the dc charge or voltage of the dc storage capacitor nearly constant so that the functioning of the system remains unaffected. This can only be done by drawing active current from the source to replenish the losses through a feedback mechanism. Therefore to put the active filter into use it is important to discuss the following issues.

- The control strategy, taking into account transient and steady states
- The high efficiency large capacity converter used as the power circuit
- The current control scheme of the converter

1.3 CONTROL ASPECTS OF ACTIVE FILTERS

The following issues are involved in the control of an active filter:

- Measurement of voltage and/or current signals

- Extraction of harmonic components
- Control of capacitor voltage
- Generation of control signals for semiconductor switches

The reference current that the compensator must follow or track is a function of the load current. However, the load current is not known a priori. Moreover, the load may also change. Therefore a suitable strategy must be employed for the extraction of the reference current. This is one of the biggest challenges in an AHCC design.

Various methods have been proposed for generating the compensator reference current. The averaging methods [11] can eliminate only the fundamental reactive power in steady state. The instantaneous p-q theory has gained considerable attention and is well-established [6]. This theory can be utilized to compensate either fluctuating or constant part of the load reactive power as well as the fluctuating part of the real power. The theory of instantaneous symmetrical components for generating instantaneous reference to balance a given load is presented in [12,13]. The instantaneous power in an unbalanced system contains an oscillating component that rides over the dc value. In this scheme the compensator supplies this oscillating power and the steady component is supplied by the source. However, in all the above-mentioned schemes the requirement of large number of transducers for measurement and intensive computation tends to make the system operation complex. A much simpler method, in which the sinusoidal reference current from the source is generated by passing the error in dc capacitor voltage through a PI controller, is proposed in [14,15]. In this thesis a simple method is proposed, in which the sinusoidal reference current that the source must supply is generated by passing the error in dc capacitor charge through a PD controller [16,17].

The basic philosophy of the scheme is to maintain the dc capacitor charge constant. In case of a PD controller, the dc capacitor charge reduces a bit from its set reference value and then is maintained constant. There is a constant steady state error. However, a PD controller eliminates any overshoot or sharp fall in the dc capacitor voltage. In a PI controller if the correction is not proper, then voltage will rise or fall monotonically. Moreover the loss in the system would be less with a PD controller. This can be explained as follows. If a PD controller is used, the dc capacitor voltage will reduce a little bit from the reference value. However, as long as the capacitor voltage is higher

than the peak of the sinusoidal voltage of the ac bus, the current flow between the source and the capacitor is bi-directional, which is essential for compensation. On the other hand, a PI controller tends to maintain dc voltage constant. Again to encompass the entire operating range of the load current, the dc voltage has to be held higher than peak of the ac voltage. Therefore the loss in this case will be more than that with a PD controller.

The philosophy of this PD controller is explained now. When the source supplies a non-linear or reactive load, it is expected to supply only the active fundamental component of the load current for an ideal lossless system. However, the inverter (compensator) would have losses due to switching in addition to the losses in the interface inductor. The outer capacitor voltage control loop would try to maintain the capacitor voltage and this is also mandatory for successful operation of the compensator. Therefore the system losses have to be provided by the source. The compensator is supposed to supply the harmonic power, which manifest itself only on the reactive component of power. Therefore under steady state operation the dc capacitor charge should remain essentially constant. In the transient conditions the load changes are reflected in the dc capacitor charge as an increase (or decrease) as capacitor absorbs (or delivers) the excess (or deficit) power. This conservation of energy philosophy is used to obtain the reference current for compensator in this method. The perturbations in the capacitor charge are related to the perturbations in the line current magnitude and perturbations in the average power drawn by the non-linear load. Therefore this perturbation in the capacitor charge is the reflection in the change of mains current. This property is utilized which facilitates extraction of compensator reference.

1.4 CONVERTER TOPOLOGIES FOR ACTIVE FILTERS

Out of the several schemes suggested in literature, the hard-switched PWM inverter based shunt compensator has gained prominence [1-2, 13-14, 18-22]. However, this compensator has its inherent limitations of high switching losses because of hard switching. This puts a constraint on the maximum switching frequency. It also requires a large dc link filter and hence its time response is sluggish. For proper current tracking,

the approximate current bandwidth is usually the PWM frequency divided by a factor of ten. Therefore, PWM based compensator fails to track high frequency components, particularly at high power level. For example, if the harmonics up to nineteenth are to be considered for a 500 kilowatt converter load, then the compensator should have a power rating of 100 kVA and it must be capable of switching at a frequency of about 9.5 kHz or higher. This is a difficult task given the current state of the art of power semiconductor device technology [23]. Without adequate current regulator bandwidth, compensation can never be perfect as there will be phase shift error and chattering in the compensated current drawn from the source [24]. Therefore current regulator limitations adds to the above mentioned problems. Additionally, the response time should be fast.

In essence, we must be able to realize a large capacity non-sinusoidal current source generator, which must follow its command instantaneously. For active harmonic current compensation, a high power topology with adequate current regulator bandwidth is necessary.

Switching losses are one of the main restrictions that is put on the high operating frequency. Using conventional switching techniques, inverters of over 10 kW are restricted to operate at frequencies of below 10 kHz [25]. If the switching frequency could be raised, important gains can be made in the areas of response time, frequency spectrum, audible noise and modular size. The limitations of PWM inverter based systems are summarized below.

- Limitations of the maximum switching frequency. This is because switching losses in the devices are directly proportional to the switching frequency.
- EMI due to high di/dt and dv/dt
- Devices with large safe operating area are needed. High device stresses may result due to recovery of feedback diodes.
- Large dc link filter
- Poor fault recovery characteristics
- Acoustic noise is generated because switching frequency lies in the audible range
- Reduced reliability due to higher heatsink temperature

Other inverter topologies also tried out for active filtering application. Active power filter using resonant pole inverters is reported in [23]. With this inverter switching frequencies of the order of 10-20 kHz at multikilowatts power levels are feasible. A current-mode modulation strategy is proposed and is seen to realize good spectral characteristics. It is seen that harmonics of order 13 and higher are eliminated, lower order harmonics reduce by 10 dB.

Active Power line conditioner using resonant converter is presented in [26]. Compensation is achieved by injecting high frequency resonant current pulses of appropriate amplitude, into the supply lines at regular sampling intervals A parallel-resonant dc link switch-mode var compensator system is simulated in [27].

In recent times multilevel inverter topologies [28] and multi-pulse [29] inverter topologies are used for active filtering application. In order to achieve high power levels, several voltage source inverters (VSIs) are connected in parallel to the dc bus. This necessitates complex transformer connections and hence makes the topology complex. Therefore recent trend shows the use of multi-level and multi-pulse inverters for active filtering. For high power applications, the multilevel inverter is preferred over the commonly used two level voltage source inverter from the standpoint of harmonics, dc link voltage and inverter switching frequency. Even though a multi-step inverter is also capable of the same, a multi-level inverter is preferred over multi-step inverters to avoid complex series-parallel connection of transformers. Moreover, because of the improved waveforms, these inverters have superior harmonic characteristics. Multilevel inverter structures and control methods are reported in [30].

Another important inverter topology is the so-called resonant dc link inverter (RDCLI). This topology offers adequate current regulator bandwidth because of high frequency operation, and hence an ideal candidate for active filtering application.

1.5. RESONANT DC LINK INVERTERS

Resonant dc link inverters promise marked gains for adjustable speed drives, power supplies and active filtering applications. Among the various types of resonant links, the parallel resonant DC link is quite attractive for implementing zero voltage switching (ZVS) [31]. This is based on shunt resonance. This inverter is quite simple in the sense

that it needs a minimum number of devices, it is easy to implement and requires simple control. Compared to a regular pulse width modulated (PWM) inverter this inverter requires an additional resonant inductor and a resonant capacitor. The resonant circuit is connected between dc source and the inverter so that the input voltage to the inverter oscillates between zero and to a value that is slightly greater than twice the dc bus voltage. The advantage of this soft-switched inverter is well known [27, 31-35]. It reduces the dominant switching losses in the inverter devices, allows higher switching frequencies at reasonably high power level and reduces noise and electromagnetic interference. Because of the minimal switching loss, the efficiency is high and cooling requirement is minimal. Additionally, the devices do not require any snubbers. Some of the advantages of this inverter are:

- The switching loss is practically zero because of zero voltage switching (ZVS).
- The frequency of operation can be very high.
- Snubber circuits are not required.
- Reliability is higher from the heat sink point of view.
- EMI is less and acoustic noise is not present.
- It has a fast transient response.

This simple topology however has few drawbacks. These are higher device voltage stresses (when the output voltage is greater than twice the dc input voltage), zero crossing failure unless the initial current in the resonant inductor is built properly. The voltage overshoot problem can be overcome by using actively clamped RDCLI [32]. Through clamping it is possible to limit the voltage stresses of the inverter devices to 1.3 to 1.8 times the dc voltage The actively clamped RDCLI circuit however has few disadvantages. The link frequency varies with variation in the dc link voltage. This manifests itself in large current jumps. This topology increases losses due to introduction of the clamping circuit. The additional clamping device increases the complexity of the power circuit and the control circuit. Moreover, the control of the clamping device becomes extremely difficult at high frequencies [33].

In this thesis the basic RDCLI is considered for power circuit of an AHCC. An important consideration for successful operation of RDCLI is that there should not be any zero crossing failure. Zero crossing of the resonant link DC voltage is mandatory in

every resonant cycle for successful operation of the inverter. Failure of resonant link tends to occur because of the finite Q of the resonant circuit where the capacitor voltage tends to build up in successive resonant cycles. Therefore an appropriate initial current must be built up in the inverter which would then ensure a zero crossing of the voltage. This must be done in every resonant cycle. The built up of fixed initial inductor current is adopted to ensure zero crossing in every resonant cycle in [31]. However, the initial current is a function of the inverter input current, which depends upon the load current of the inverter. In a practical circuit, the load current would fluctuate and hence the load current seen by the resonant link can be bi-directional. Thus using a fixed initial inductor current concept would not ensure zero crossing in every resonant cycle unless this current is designed on the worst case basis. This approach however would aggravate the voltage overshoot problem. A programmable initial current control technique for RDCLI was reported in [34-35]. This scheme is somewhat complex from the implementation viewpoint. A current prediction scheme is proposed in [33] for finding out the initial current. The functioning of the link depends on the detection of the zero crossing of the resonant capacitor. This scheme requires a sensitive detection of zero voltage crossing.

In this thesis we present a new current initialization technique [24,36] for the resonant circuit which ensures reliable zero voltage switching. The proposed method is based on state transition equation and is simple to implement. The equivalent circuit of a RDCLI is shown in Fig. 1.2. This contains a resonant circuit generated by an inductor (L) and a capacitor (C) as shown in this figure. The inductor coil has a resistance (R) due to its finite Q-factor. The voltage (v_C) across the capacitor is called the dc link voltage. Using the resonant circuit properties, this voltage goes through zero periodically. The switch (S_0) shown in Fig. 1.2 represents the switch across the link. This switch is required to short the link when the voltage v_C is zero for the current i_R to build up. The current i_0 is the input current of the inverter, this acts as the load current for the resonant link. It is assumed that the current i_0 remains constant during a resonant oscillation period. Therefore this current is indicated by the current source I_0.

The philosophy is to switch the device only when the voltage across it is zero. For a given set of resonant link parameters, a constant resonant oscillation period is selected. The state vector consists of link capacitor voltage (v_C) and inductor current (i_R) in Fig. 1.2. The capacitor voltage must be zero at the start and at the end of every resonant oscillation period for successful ZVS. With this condition, the exact initial value of the inductor current (i_R) is determined. In order to start a resonant cycle with this value of the initial current, the time duration for which the dc bus must be shorted can be calculated. Thus, the initial inductor current is generated by shorting the link and a resonant cycle commences with proper values of capacitor voltage (zero) and inductor current. This forces the link capacitor voltage to return to zero after a pre-specified resonant oscillation period.

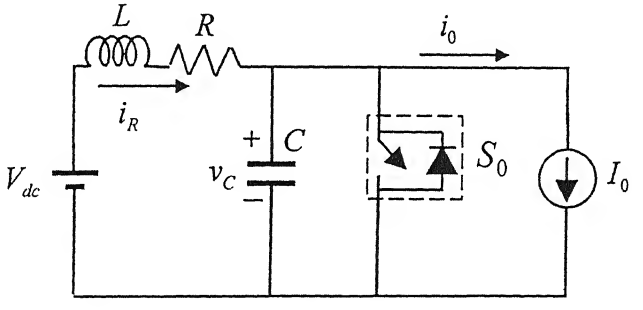


Fig. 1.2 Equivalent circuit of an RDCLI

The philosophy of using this soft-switched inverter is to obtain a high current regulator bandwidth as desired. This topology would offer adequate current regulator bandwidth for compensating higher order harmonics because of high frequency switching. Furthermore, this compensator can achieve high efficiency by reducing switching losses. Moreover, the transient response is fast and the control is simple.

The control of RDCLI is different from the conventional PWM inverter [37-39]. The switching of the devices are carried out when the voltage across the link is zero to achieve ZVS. The current control in this inverter is done through zero-hysteresis bang-bang control. The basic difference from the PWM schemes is the existence of pre-specified permitted switching instants. No computations are necessary for specifying a pulse width. The only decision that needs to be made is which inverter state is to be

selected. This decision can be made based on current error (feedback signal). The inverter state selection is done to achieve current regulation objectives.

This compensator is capable of compensating lower as well as higher order harmonics at a reasonably high power level (1 MVA to 2.5 MVA level distribution system) where a PWM inverter based harmonic compensator finds limitations because of inadequate current regulator bandwidth.

1.6 OBJECTIVE OF THE THESIS

The extensive use of non-linear loads results in harmonic pollution in a power distribution system. This leads to waveform degradation in power supply networks. A number of techniques have been suggested in the literature for compensation of line current harmonics. However, all these schemes suffer from one or more drawbacks such as load dependence, large system size, inadequate current regulator bandwidth, poor system efficiency and complexity of control.

Keeping in view of the above considerations we define the following objectives of the thesis.

1. To find out a suitable topology for AHCC such that the compensator would achieve high efficiency, provide adequate current regulator bandwidth and fast transient response.
2. To devise a suitable control strategy for the extraction of compensator current reference.
3. To study the different control aspects of the AHCC such as current regulation within the inverter and any other control required for the inverter.
4. To evaluate the performance of the AHCC in terms of compensation, response time, efficiency etc. through simulations and experiments.

1.7 OUTLINE OF THE THESIS

Chapter 2 begins with a discussion on multilevel inverter and more specifically on a three-level inverter. We then discuss a three-level inverter based active harmonic current compensator. A closed-loop model in conjunction with PD controller is proposed for extraction of compensator reference. The performance of this compensator

in conjunction with the PD controller is evaluated. The compensator is able to compensate load harmonics and has a fast transient response. However, in the presence of unbalance in the load, the circuit response becomes slow. All the above points are demonstrated through digital simulation.

In Chapter 3 we demonstrate the use of a soft-switched RDCLI as an AHCC. A new current initialization scheme is proposed that ensures ZVS. The performance of this topology as an AHCC is investigated. The current control in the inverter is done through zero-hysteresis bang-bang control. The inverter switching state selection is done to achieve regulation objectives. This compensator performs reliably for balanced load conditions. However, its performance degrades under unbalanced load conditions because of the unconnected neutral. These points are highlighted in this chapter.

In Chapter 4 single-phase hard-switched inverter based AHCC is considered. Two control strategies are discussed for extracting the compensator reference. As shown through digital simulation, the performance of the compensator is quite good.

In Chapter 5 we consider two different soft-switched inverter topologies that can be used single-phase AHCC. First the performance of the RDCLI based on the current initialization technique described in Chapter 3 is investigated, vis-a-vis its switching frequency and dc voltage level. Next we consider a quasi-resonant dc link inverter (QRDCLI) based AHCC. It is shown that a QRDCLI based AHCC, even though more complex than an RDCLI based AHCC, does not have an improved performance over the RDCLI based AHCC. All these are demonstrated through simulation studies. Further a topology for three-phase AHCC is also proposed in which three single-phase RDCLI that are driven from a single dc storage capacitor is used as power circuit. Simulation results show that this topology offers much improved performance than a three-phase RDCLI based AHCC.

In Chapter 6 experimental setup for the single-phase RDCLI based AHCC and PWM inverter based AHCC is described. Details of the power circuits, various control circuits and PC interface are presented. The use of PC for the current initialization makes the circuit simpler and flexible.

In Chapter 7 we present the experimental results obtained in the laboratory through lab prototypes. For purpose of comparison, some further simulation results for load cases identical to those in experimental setup are also obtained. The experimental results

are in close agreement with the theoretical results obtained in the earlier chapters thus validating the concepts presented in this thesis.

In Chapter 8 the general conclusions derived from this thesis are presented. This chapter also presents some future directions for research in the area of AHCC.

CHAPTER 2

THREE-LEVEL INVERTER BASED ACTIVE HARMONIC CURRENT COMPENSATOR

Active Filtering plays an important role in reducing harmonics in a power distribution system. Shunt active power filters employing two level voltage source inverters have been proposed in the literature [13-15,18-22]. These equipment are used to compensate for power factor and current harmonics in distribution systems. Because of the restricted power handling capabilities of the power semiconductor devices, these types of active power filters are usually connected through a coupling transformer to match the source voltage.

Among various VSI topologies the multi-phase and multi-level configurations are quite popular for high power applications. The multi-phase configuration requires rather complex transformer connection [29]. Multi-level inverters are quite suitable for active harmonic current compensation application and offer several advantages that are discussed in this chapter.

An active harmonic current compensator (AHCC) is implemented using a three-level inverter. A simplified closed-loop model is proposed for this AHCC employing a three-level inverter. Although PI and PD controllers for the proposed model have been investigated, the later controller is found to offer better performance. This model makes it possible to extract instantaneous active fundamental component of the load current. The proposed control strategy is quite simple and offers overall excellent performance.

We begin this chapter by reviewing a three-level inverter. The superior features of this topology for AHCC application are discussed. The suitability of the proposed closed-loop model and PD controller for extraction of fundamental component of the

load current is demonstrated vis-a-vis a comparison with PI controller. Compensation is achieved by injecting compensating currents into the source to cancel the harmonics in the load current. The current control is achieved using standard hysteresis current control. The performance of the AHCC together with the proposed model is validated through extensive simulation results.

2 .1 MULTILEVEL INVERTER

For high power applications, the multilevel inverter is preferred over the commonly used two level voltage source inverter from the standpoint of harmonics, dc link voltage and inverter switching frequency. Even though a multi-step inverter is also capable of the same, a multi-level inverter is preferred over multi-step inverters to avoid complex series-parallel connection of transformers. Moreover, because of the improved waveforms, these inverters have superior harmonic characteristics. Multi-level inverter structures and control methods are reported in [28, 30, 40-43]. As the numbers of levels are increased, the switching frequency is to be reduced. In the present study an AHCC using a three-level inverter as shown in Fig. 2.1 is considered.

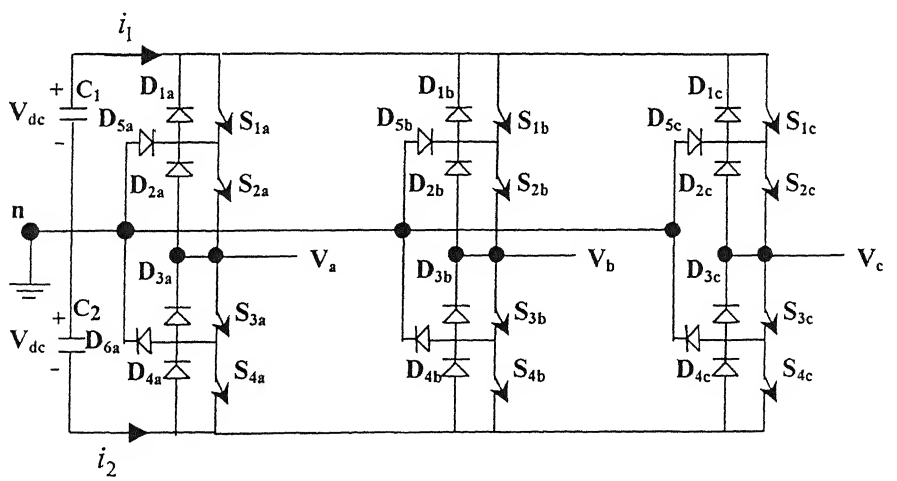


Fig. 2.1 Structure of a three-level inverter

A three-level inverter offers several advantages over a two-level inverter. The blocking voltage of each switching device is one half of dc link voltage compared to full dc link voltage for the two-level inverter. Three-level PWM inverters can be directly connected to high voltage source without a coupling transformer. This inverter can be

directly coupled to 3.3 kV system ac mains using suitable devices of higher voltage rating. The harmonic contents of a three-level inverter output voltage is quite less than those of a two level inverter for the same switching frequency. Hence a three-level inverter can be operated at a lower switching frequency without excessive harmonic currents. The clamping of neutral point in these inverters allows equal voltage sharing of the series connected devices in each phase. The above superior features make a three-level inverter a suitable candidate to work as a harmonic compensator.

A three–level inverter structure is briefly reviewed below. For the sake of clarity, only one leg of a three-level inverter is shown in Fig. 2.2. It has four switches with their anti-parallel diodes. We denote each switch and its anti-parallel diode as a group. Table. 2.1 shows the status of switches for various output voltage levels. This configuration can be easily extended to more number of levels by adding switches and capacitors suitably.

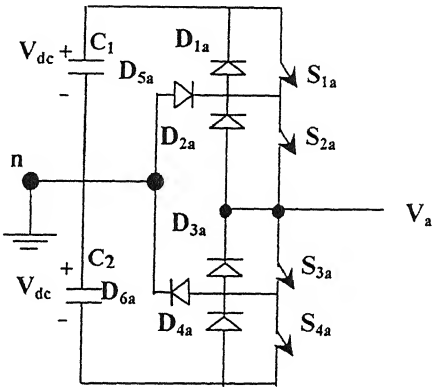


Fig. 2.2 Schematic diagram of one leg of three level inverter

Table.2.1. Status of switching devices

V_a	$+V_{dc}$	O	$-V_{dc}$
S_{1a}	ON	OFF	OFF
S_{2a}	ON	ON	OFF
S_{3a}	OFF	ON	ON
S_{4a}	OFF	OFF	ON

2.2 PRINCIPLE OF AHCC

An AHCC must be able to perform the following functions

- Provide reactive power to the load
- Correct the power factor of the source

- Balance an unbalance load

Fig. 2.3 shows the schematic diagram of an AHCC. The dc side of the AHCC is connected to an energy storing capacitor and the ac side of the inverter is connected to ac bus through a filter inductor. The point (p) at which the AHCC is connected to the power system is called the point of common coupling. This ac bus supplies various loads including the nonlinear ones. The compensator is controlled in a closed-loop manner—the inverter switches are controlled to actively shape the current through the inductor following a command current such that the input current from the source is in phase and of the same shape as the input sinusoidal voltage. The compensator supplies reactive and harmonic components of the load current and hence the source will be required to supply only the in-phase fundamental component of the load current.

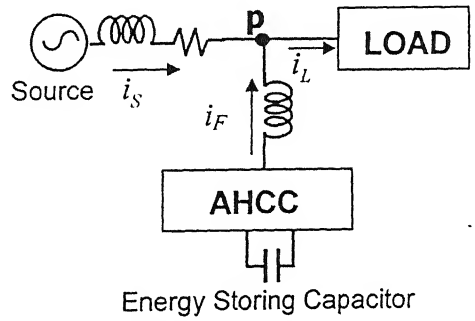


Fig.2.3 Schematic diagram of AHCC

The reference current that the compensator must generate is a function of the load current. However, the load current is not known a priori. Moreover, the load may also change. Therefore a suitable strategy must be employed for the extraction of these currents. This is one of the biggest challenges in an AHCC design.

Different approaches have been adopted in the literature for the extraction of compensator reference current(s) using voltage and/or current measurements. These methods are averaging technique [11], p-q theory [6], instantaneous symmetrical component theory [12-13] etc. The averaging techniques have the limitations in the sense that it can eliminate reactive power in steady state only. P-Q theory and instantaneous symmetrical component methods require a large number of sensors and are computationally intensive. A much simpler method, in which the sinusoidal reference current from the source is generated by passing the error in dc capacitor voltage through a PI controller, is pro-

posed in [14-15]. The main drawback of the scheme is that the proportional and integral gains are chosen heuristically. The closed-loop model of the AHCC presented in this thesis would facilitate control design to achieve several control objectives [16].

In this chapter a closed-loop model of the AHCC based on the charge balance of the energy storing capacitor is proposed. A PD controller is an integral part of this model. It is shown that this controller is a natural control law for this system and it offers excellent performance. The proposed model permits extracting the instantaneous active fundamental component of the load current even under adverse load conditions. However, we shall also investigate the effect of a PI controller on the system.

2.3 PROPOSED MODEL

In this thesis, we propose a feedback model of the current compensator. This is shown in Fig. 2.4. The output of the AHCC model is the sum of total charges of the two dc storage capacitors (C_1 and C_2 of Fig. 2.1). We denote this by q_{meas}. This is obtained by integrating the capacitor currents i_1 and i_2. These currents are given by

$$\left.\begin{aligned} i_1 &= S_1 i_a + S_3 i_b + S_5 i_c \\ i_1 &= -(S_4 i_a + S_6 i_b + S_2 i_c) \end{aligned}\right\} \qquad (2.1)$$

where i_a, i_b and i_c are the phase currents and the switching functions are given by S_1 through S_6. The switching function S_1 assumes a value of 1 when switches S_{1a} and S_{2a} are on; otherwise it will assume a value of zero. The switching function S_4 will assume a value of 1 when S_{3a} and S_{4a} are on, otherwise it will take the value zero. These two switching functions take care of phase-a. Similarly S_3 and S_6 will decide the switching action of phase-b, S_5 and S_2 for the phase-c. This nomenclature S_1 through S_6 is done for convenience and in consistency with the inverter literature. Depending on the voltage level chosen, particular pair of switches needs to be on. Moreover because of neutral clamping, a particular phase during a switching condition gets connected either to capacitor C_1 or capacitor C_2. In such a case, the capacitors either absorb or deliver power from that particular phase. However, the total charging or

discharging will depend on all three phases. It may so happen, that during a particular switching condition, one capacitor gets connected to particular phase(s) only. Furthermore, if zero voltage level for the three-level inverter is chosen for a particular phase, that phase will not contribute to charging or discharging of either capacitors.

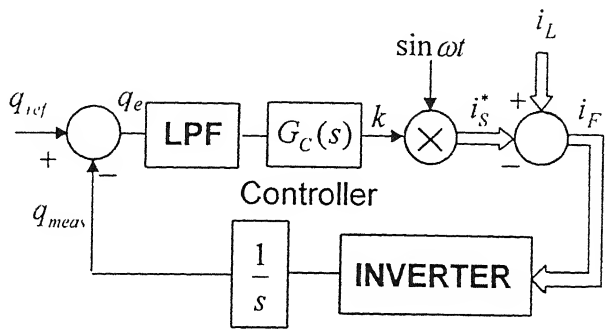


Fig. 2.4 Block diagram of the proposed closed loop model with proposed PD controller.

The measured value of the charge is then compared with the charge reference q_{ref}. The error q_e is then passed through a low pass filter (LPF) to eliminate high frequency ripple due to switching. The cut-off frequency of the LPF has to be chosen such that unwanted high frequency components do not appear at the controller side, while at the same time it should not slow down the controller response. The output of the LPF is passed through a controller. The controller output is multiplied with a template of source current to generate the source reference current i_S^*.

It is to be noted that for a three-phase circuit we used three such reference currents. In such case, three differential templates, that are phase shifted by 120° and are in phase with the corresponding voltages are required. It can be seen from Fig. 2.3 that KCL at the point of common coupling yields

$$i_F = i_L - i_S \tag{2.2}$$

Hence once i_S^* is obtained, it is subtracted from the load current of the corresponding phase and the resultant is used for generating the reference compensating current. This current is then tracked in a hysteresis band current control mode (or for that matter any other current control mode).

The controller $G_c(s)$ can be a proportional plus integral (PI) controller. However, as the basic purpose is to hold the charge constant, a small non-zero value of q_e may force the integral control to monotonically increase. On the other hand, a current can be obtained by differentiating the charge. Thus a derivative controller is the most natural in this case. Thus, the current reference is obtained by differentiating the error in charge. However, a pure differentiator is normally avoided to reduce noise. Therefore, a PD controller is used instead. Again, a purely differential controller sK_D is not quite practicable [44]. Thus, a PD controller of the form

$$G_C(s) = K_p + \frac{sK_D}{1 + s\frac{K_D}{N}} \tag{2.3}$$

is used where K_p *and* K_D are the proportional and differential gains respectively and N is a constant usually chosen between 3 and 20 [44]. The transfer function of the block diagram of Fig. 2.4 can be obtained and the choice of values of K_p and K_D can be studied depending upon the control objectives. It is observed that a higher value of K_p improves the response time of the compensator. But it may introduce distortion. The transfer function of the LPF is given by

$$G_L(s) = \frac{\omega_n}{s + \omega_n} \tag{2.4}$$

The frequency response curves of this model with PD and PI controllers are shown in Figs. 2.5 and Fig.2.6 respectively. It is to be noted that the frequency response plots are drawn for the LPF and respective controllers only. The parameters chosen are

- PD Controller: $K_p = 100$, $K_D = 40$, $N = 20$
- PI Controller: $K_p = 200$, $K_I = 20$
- LPF: $\omega_n = 377$ rad/s

The gain and phase margins obtained with the PD controller are 81.94 dB and 73.05 degrees respectively while those obtained with PI controller are 76.81 dB and 57.85 degrees respectively.

It can be seen that both these stability margins are better with PD controller. This implies that the system is more stable and has good time response. In order to achieve different control objectives such as faster response, better stability margin etc., these design curves can be utilized. As mentioned earlier, the response can be made faster by increasing the value of K_p. With an increase in the value of K_p the system response becomes faster. This is depicted in Fig, 2.7. The responses of the PD controller when used in conjunction with an AHCC, with three different values (50, 100, 200) of K_p are shown. It is clear that response time improves with an increase in K_p. However, the control effort is also increasing. This results in distortion in the reference current. Also, as mentioned before, the cut-off frequency of the LPF has a major role in the response time-thus this frequency and the choice of K_p play a vital role in successful implementation of AHCC.

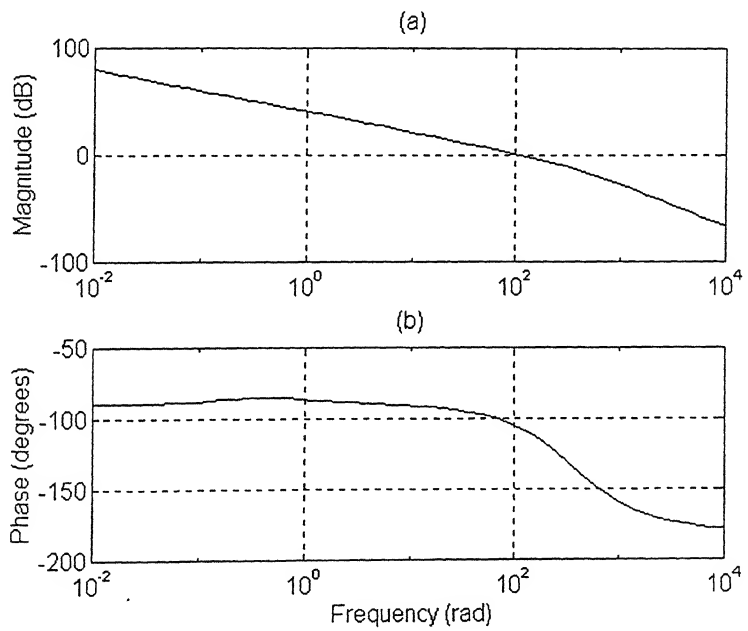


Fig. 2.5 Frequency response with PD controller (a) Magnitude (b) Phase

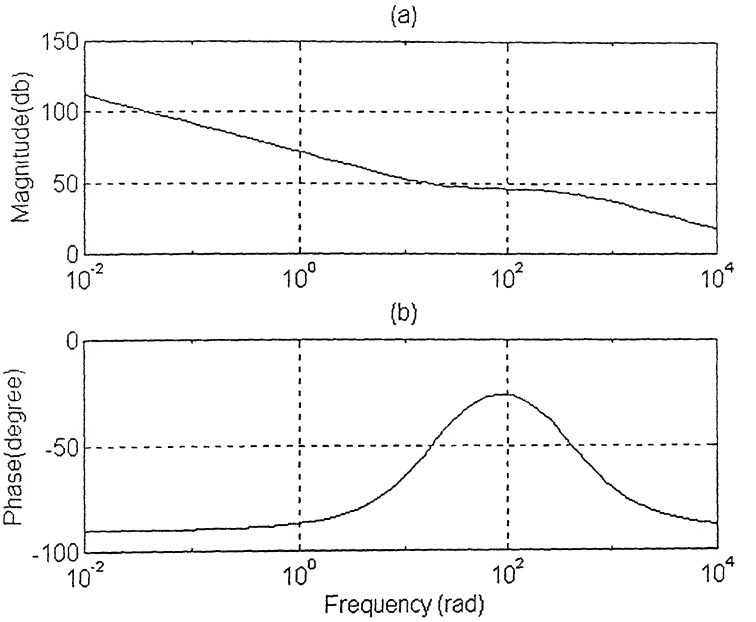


Fig.2.6 Frequency response with PI controller: (a) Magnitude (b) Phase

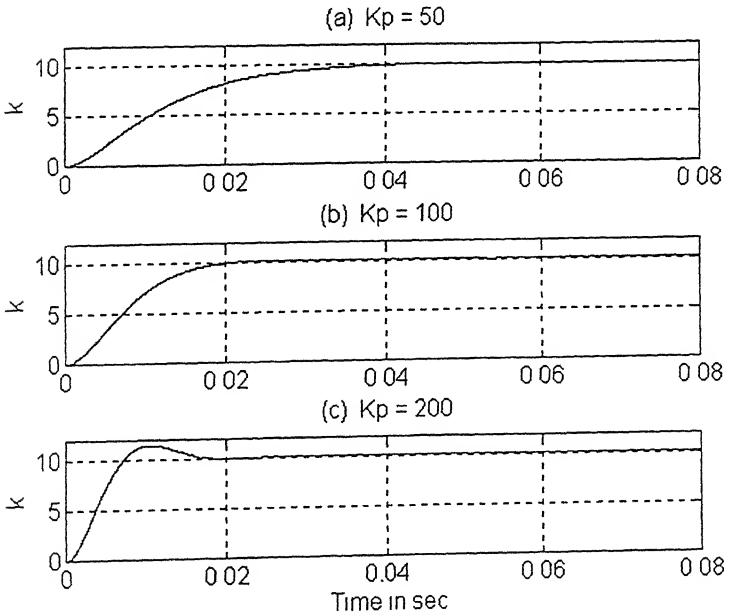


Fig.2.7 PD controller response with different values of Kp (a) K_p =50, (b) K_p =100 and (c) K_p =200

2.4 SIMULATION RESULTS

In order to evaluate the performance of the AHCC using the proposed model and controller, simulation studies are carried out. The following parameters are chosen for the simulation studies.

- AHCC and Interface circuit: $C_1 = C_2 = 2000$ μF, $L_F = 15$ mH, $R_F = 0.2\Omega$
- AC Supply: System Frequency = 50 Hz, Source Voltage = $440\sqrt{2/3}\sin(100\pi t)$
- PD Controller: $K_p = 100$, $K_D = 40$, $N = 20$, $q_{ref} = 2$ Coulombs
- PI Controller: $K_p = 200$, $K_I = 20$, $q_{ref} = 2$ Coulombs
- LPF: $\omega_n = 377$ rad/s
- Bang-Bang Current Controller: Hysteresis Band = 0.5 A

Three different tests are performed. They are:

- Power factor correction for an inductive load
- Harmonic compensation when the load is non-linear
- Balancing the supply side current when the load is unbalanced

In all these cases it is assumed that the load is star connected and its neutral point is connected to the neutral point of the three-level inverter (point 'n' in Fig. 2.1). The three level VSI is operated in the hysteresis current control mode so as to generate the desired reference currents. This is done using hysteresis control with a band of 0.5 A so that the average switching frequency is limited to 7 kHz.

2. 4. 1 Power Factor Correction

The load is assumed to be balanced but has a lagging power factor. The AHCC has to inject currents such that the supply side power factor is unity. The results are depicted in Fig. 2.8 and 2.9 with PD controllers. The output of PD controller is shown in Fig.2.8 (a). It is clear that the controller along with the low pass filter introduces a delay of 20 ms, which is one cycle in a 50 Hz system. The total charge in the capacitor is shown in Fig. 2.8 (b). It is clear that following the starting transient the total charge becomes con-

stant in steady state. The settling time is about one cycle. This indicates the effectiveness of the controller. Fig. 2. 9 shows the following

- Phase-a source voltage, scaled down by a factor of twenty such that its magnitude is comparable to the source current.
- Load Current of phase a.
- Source current of phase a.

It is observed that the source current is in phase with the phase voltage indicating the power factor correction property of the compensator.

Similar results are obtained using a PI controller as well. These are shown in Fig. 2.10 and 2.11. The controller output is shown in Fig. 2.10 (a). The controller takes about 7 to 8 cycles to settle. This is also clear from Fig, 2.10 (b) where the total charge in the dc capacitor is shown. It is to be noted that the steady state error in this case is zero. Fig. 2.11 shows the source voltage (scaled down by a factor of twenty) of phase-a along with the compensated source current of phase-a and the load current of phase-a. Power factor correction is achieved.

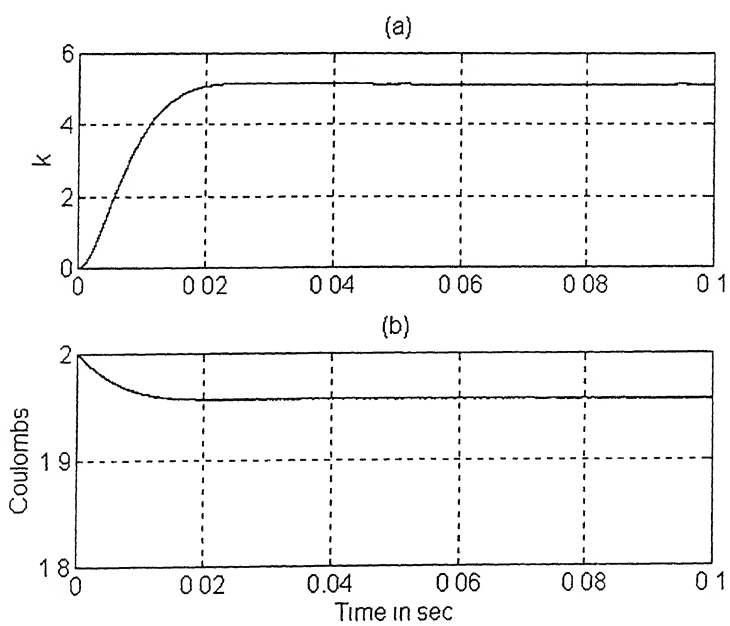


Fig. 2.8 (a) PD controller output, (b) Total charge in the dc capacitor

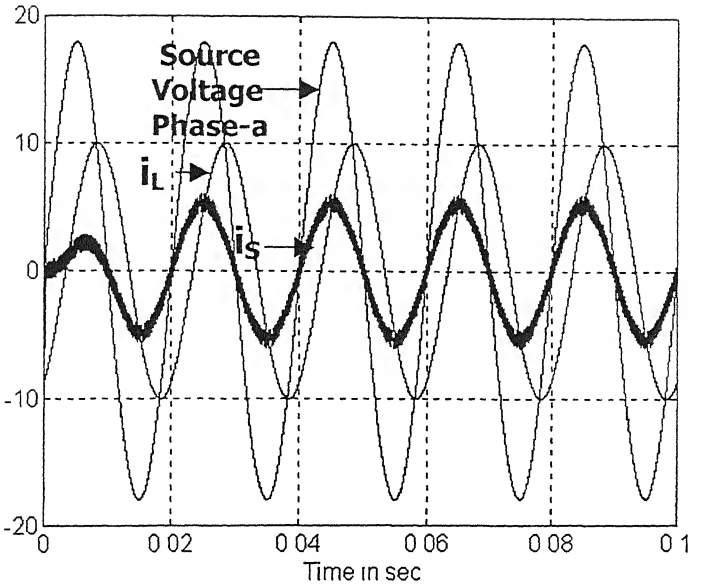
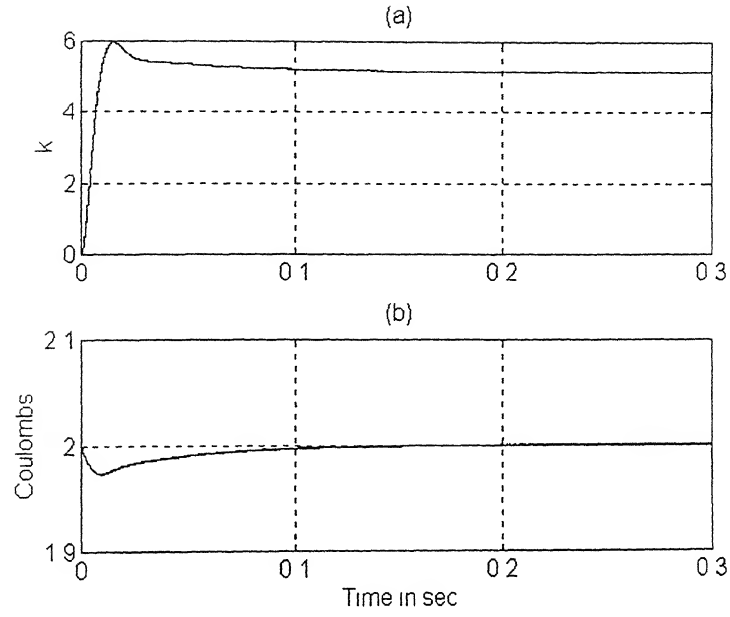


Fig. 2.9 Compensated phase-a source current, load current and phase-a source voltage (scaled down by a factor of ten)

We now bring out a comparison in the performance of the two controllers. The following observations are made

- The PD controller is faster as its response time is one cycle compared to 7 to 8 cycles in the PI controller.
- The losses in the AHCC increase with PI controller. It is observed that the controller output is higher in the case of PI controller. The source is required to supply the active fundamental components besides the losses in the AHCC. Therefore a higher current from the source indicates increased losses. This happens as the dc capacitor voltage reaches its steady state at a lower value in the case of PD controller. However, this does not affect the function of the AHCC capacitor voltage is still maintained at a higher value compared to the peak of the source voltage.



Fig, 2.10 (a) PI controller output, (b) Total charge in dc capacitor

2. 4. 2 Harmonic Compensation

The basic purpose of the AHCC is to compensate the line current harmonics. To investigate, a load current is simulated which contains 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th} harmonics other than the fundamental component. The magnitudes of these harmonic components are assumed to be inversely proportional to the harmonic number. Such currents will be drawn from the source in the absence of the AHCC. These currents are depicted in Fig. 2.12 for the three phases. For this case we study the effects with PD controller only. The controller output is shown in Fig. 2.13 where it is seen that the controller settles within 1 cycle.

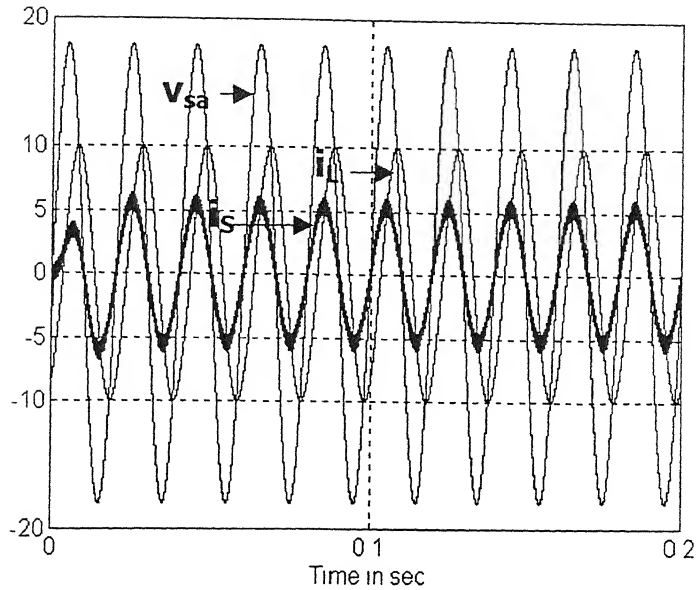


Fig. 2.11 Compensated phase-a current, phase-a load current, Phase-a source voltage scaled down by a factor of twenty

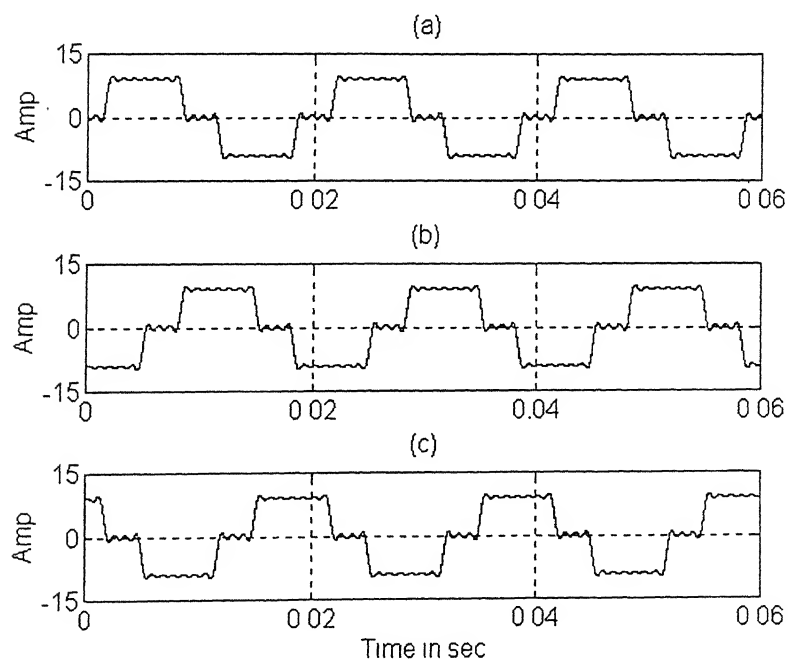


Fig 2.12 Simulated load current waveforms for phases 'a', 'b' and 'c' are shown in (a), (b) and (c) respectively

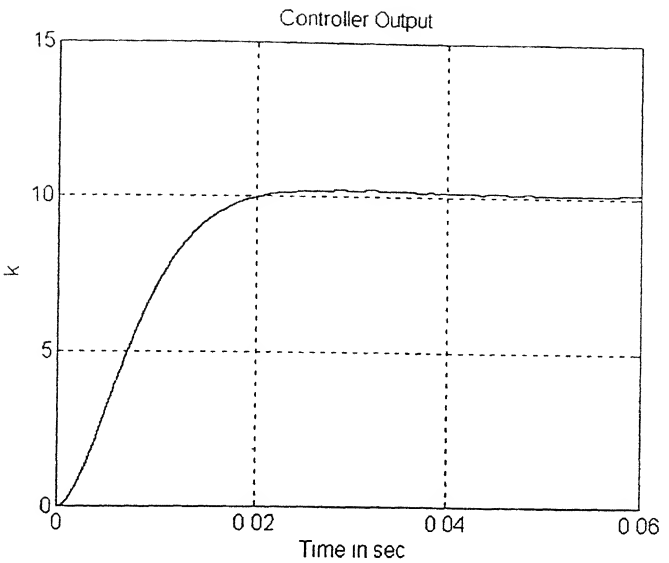


Fig 2.13 Output of PD controller ('k')

The AHCC reference currents (i_F^*) is obtained subtracting the source reference currents (i_S^*) from the load currents (see equation 2.2). The inverter is constrained to supply these reference currents. The AHCC reference current (i_F^*) and the actual inverter output current i_F are shown in Fig. 2.14 (a) for phase-a. The same waveform is depicted for just one cycle for clarity in Fig. 2.14 (b). It is seen that inverter is capable of tracking this current. This figure clearly demonstrates the hysteresis control action. As mentioned before a hysteresis band of 0.5 A is chosen, to restrict the switching frequency to 7 kHz. This is evident from Fig. 2. 15 in which phase-a of the inverter voltage is shown. The inverter is forced to operate at this high frequency in order to get a better tracking. It will be shown later that at a low switching frequency it is difficult to track the reference waveform as this waveform contains high frequency fast changing components.

The compensated source currents in the three phases are shown in Fig.2.16. It is seen that the source currents after compensation are almost sinusoidal with some high frequency ripple caused due to high frequency switching. It is needless to say that the source power factor is unity. The capacitor voltages are shown in Fig. 2.17 (a) and (b), while the total charge is shown in Fig. 2.18. From these figures it is evident that these quantities settle within a cycle and is maintained thereafter. This proves the efficacy of the controller.

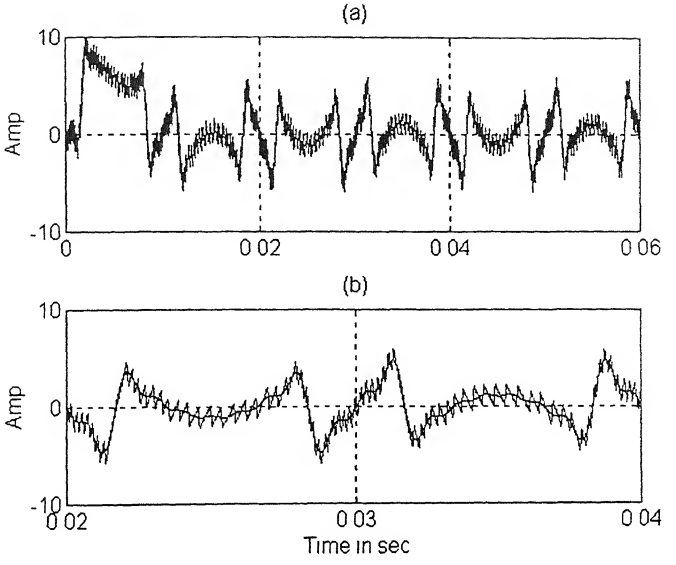
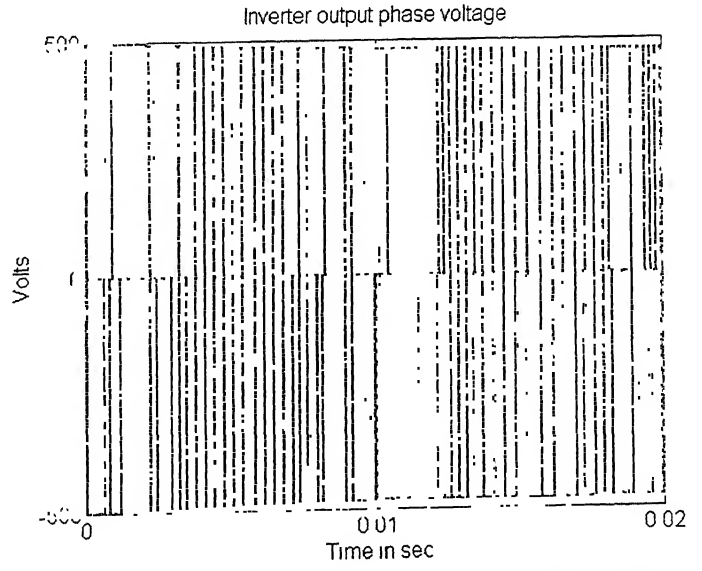


Fig. 2.14 (a) Compensator reference and tracking for phase -a, (b) Same waveform in an expanded scale

The above results are obtained when the inverter is switched at a frequency of 7 kHz. Under this condition the AHCC eliminates harmonics upto 19^{th}. To investigate the compensator performance at a lower switching frequency, the inverter is switched at 4.2 kHz with a hysteresis band of 1A. The compensated source current for phase-a is shown Fig. 2.19 (b) for this switching condition. The source current for the previous case (inverter switched at 7 kHz) is also shown in Fig. 2.19 (a) such that the two results can be compared. It is clear that the AHCC performs better when the inverter operates at a higher frequency.



Fig, 2. 15 Inverter output voltage of phase-a shown for one cycle

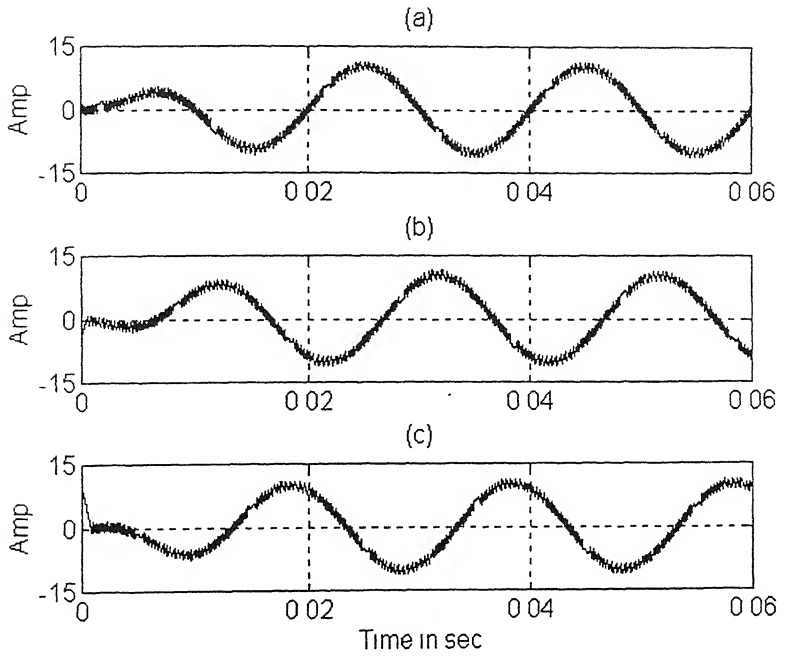


Fig. 2.16 Source currents in phases-a, b and c after compensation

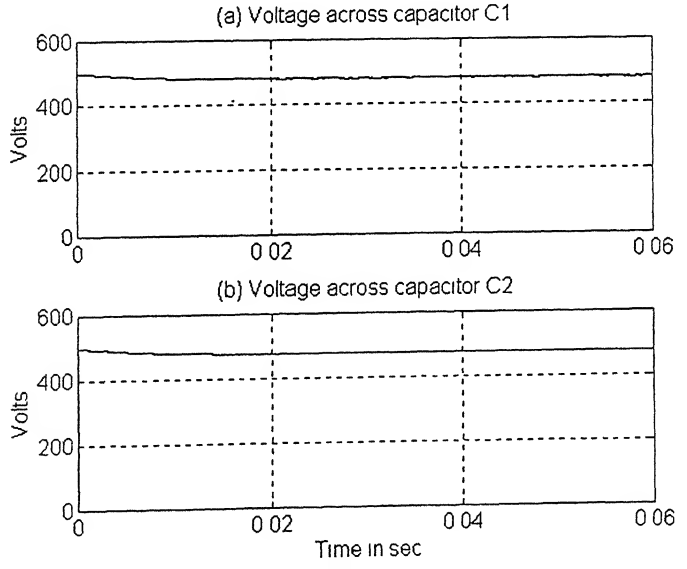


Fig. 2.17 The dc voltages across capacitors C1 and C2

The transient response of the AHCC is shown in Fig. 2.20. The load current of phase-a is shown in Fig. 2.16 (a) where the load is subjected to changes after 3 cycles and 6 cycles. The load current is suddenly halved after 3 cycles and is restored to the nominal value after 6 cycles. The compensated source current in phase-a is shown in Fig. 2.20 (b). It is observed that the source follows the load transients and settles to new

desired value after 1 cycle. The controller output and the total charge on capacitors is shown in Fig. 2.20 (c) and (d) respectively. The hysteresis band for this case is chosen as 0.5 A.

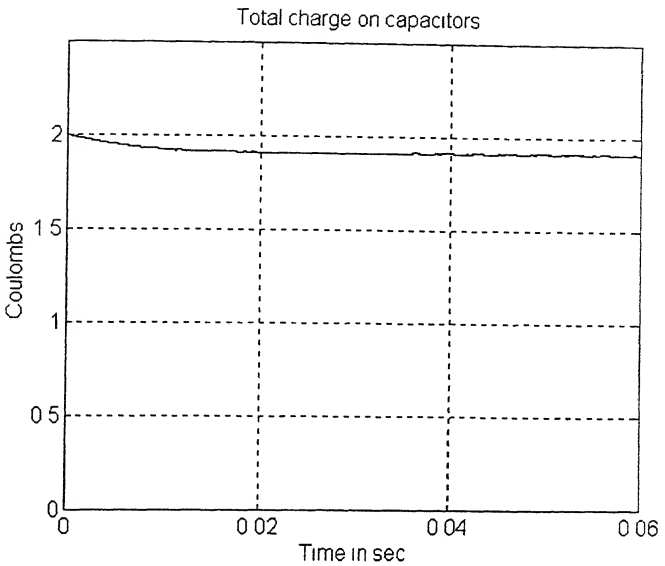


Fig. 2.18 The total charge on capacitors C1 and C2

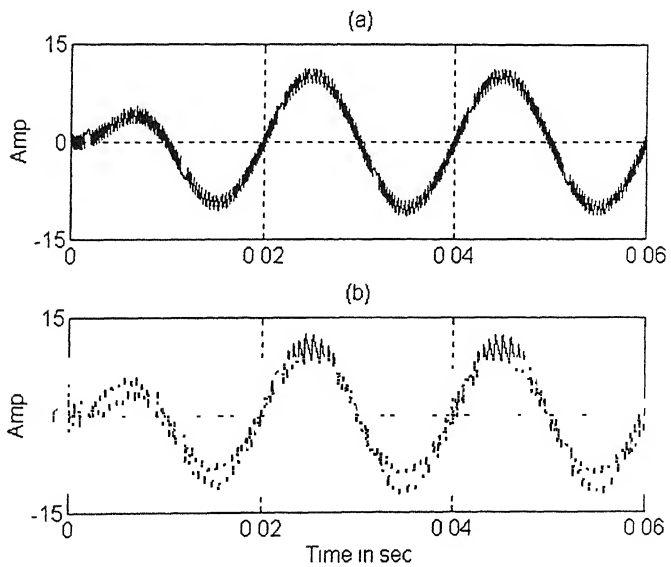


Fig. 2.19 Compensated currents from source at two different frequencies

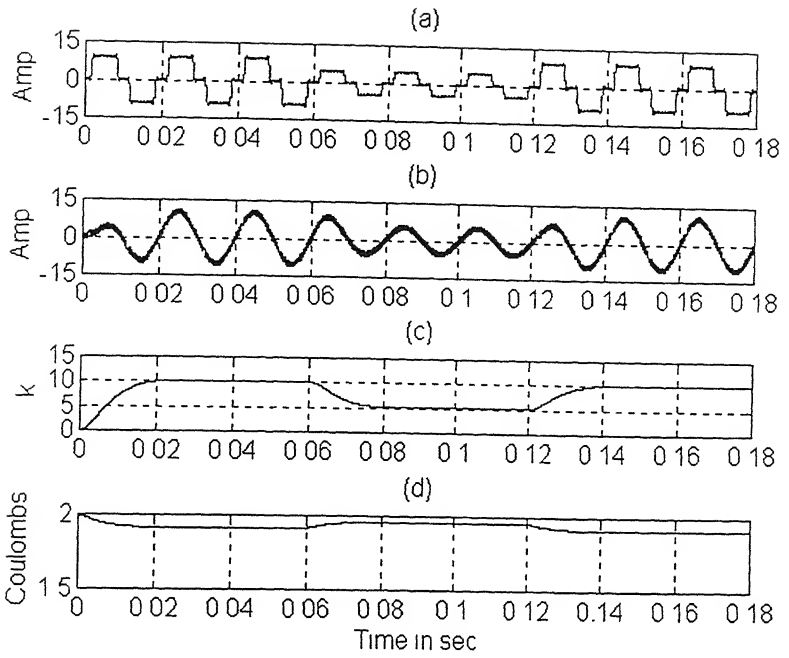


Fig. 2.20 Transient response (a) Load current (b) Compensated source current (c) Controller output and (d) Total capacitor charge

2. 4. 3 Load Balancing

A much worse load is now considered in which the AHCC has to do harmonic suppression and load balancing. The load is severely unbalanced with two phase carrying 10 A (peak) current while the third phase is open (i.e., zero current). These currents contain harmonics upto 19th order. The two non-zero load currents are shown in Fig. 2.21 (a-b). The phase difference between these currents is maintained at 120°. Because of the presence of harmonics and huge unbalance there is a large ripple in the capacitor charge. Therefore to eliminate these ripple the cut-off frequency f_n ($\omega_n = 2\pi f_n$ rad/sec) of the LPF is lowered. Naturally this slows down the response. However, the compensation is achieved after some delay. To investigate this effect the output of LPF plus controller is shown in Fig. 2.22 and 2.23 for PD and PI controllers respectively. Four different values of LPF cut-off frequency are considered for both the controllers for comparison purpose. The cut-off frequencies chosen are 120, 60, 20 and 10 Hz, and their effects are shown in these figures. It is clear that with a cut-off frequency of 10 Hz the PD controller output settles in about 12 to 13 cycles. The PI controller output does not settle within this time. The PI controller takes about 50 cycles to settle.

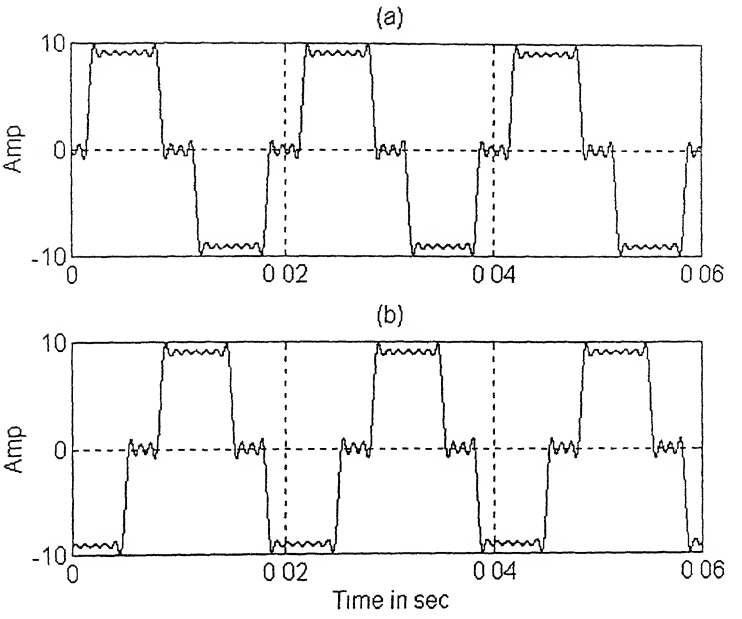


Fig.2.21 Simulated load current under unbalanced condition

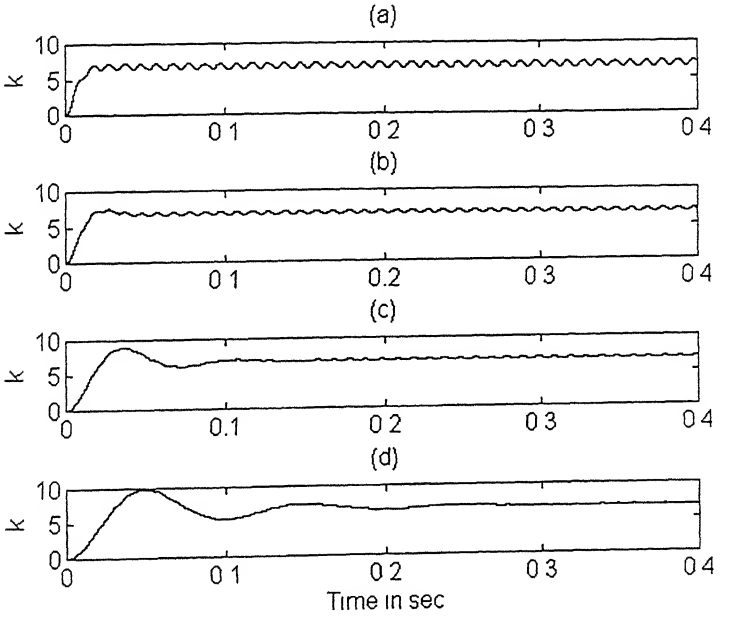


Fig. 2.22 LPF plus PD controller output at different cut-off frequency (f_n) of the filter (a) 120, (b) 60, (c) 20 and (d) 10 Hz.

The reference source currents with PD controller are shown in Fig. 2.24. (a) for all the three phases. This figure also indicates that the source currents become balanced after 12 to 13 cycles. To bring further clarity the reference currents of the source is shown for 2 cycles (14^{th} and 15^{th}) in Fig. 2.24 (b). The reference currents of the source in the presence of a PI controller are shown in Fig. 2.25. It is seen that response is too slow

and the source currents settle in about 50 cycles. For better clarity these currents are shown for two cycles (30^{th} and 31^{st}) in Fig. 2.26. It is clear that even after 30 cycles the unbalance is not cleared by the compensator. The ripple in the capacitor charge with PD controller is shown in Fig. 2.27. It can be seen that the ripple is at twice the fundamental frequency and is low in magnitude. Therefore though the charge settles the double line frequency harmonic is still reflected in it. The compensated source currents are balanced and are shown in Fig, 2.28. This result is with the PD controller.

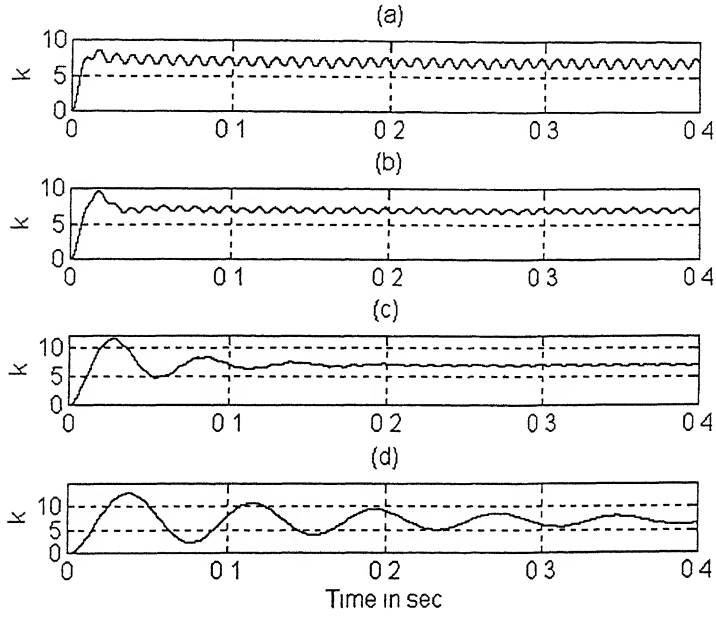


Fig. 2.23 Output of LPF plus PI controller with different cut-off frequency (f_n) of LPF (a) 120, (b) 60, (c) 20 and (d) 10 Hz.

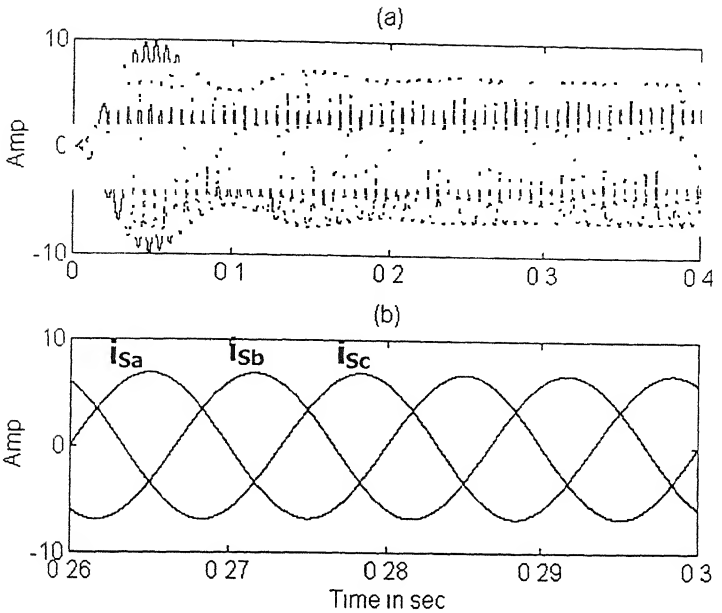


Fig. 2.24 (a) Source current references with PD controller under unbalanced load condition, (b) same waveform for 14^{th} and 15^{th} cycle

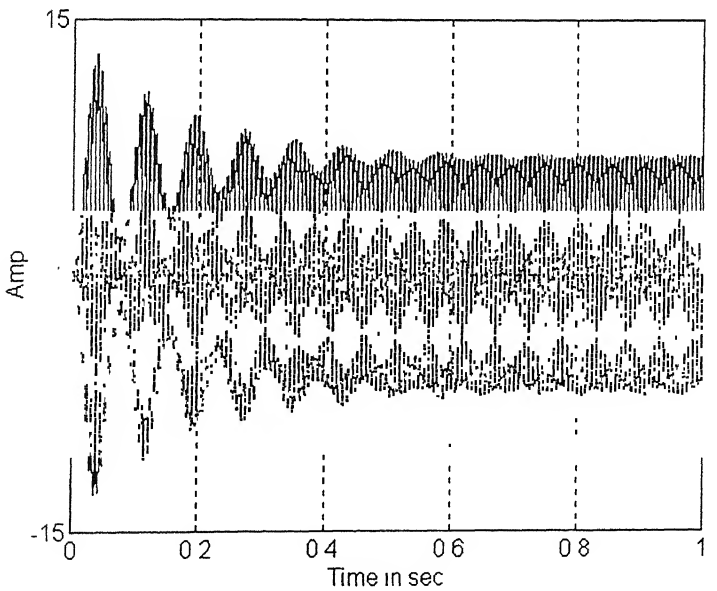


Fig. 2.25 Three-phase reference currents of the source under unbalanced loading with PI controller

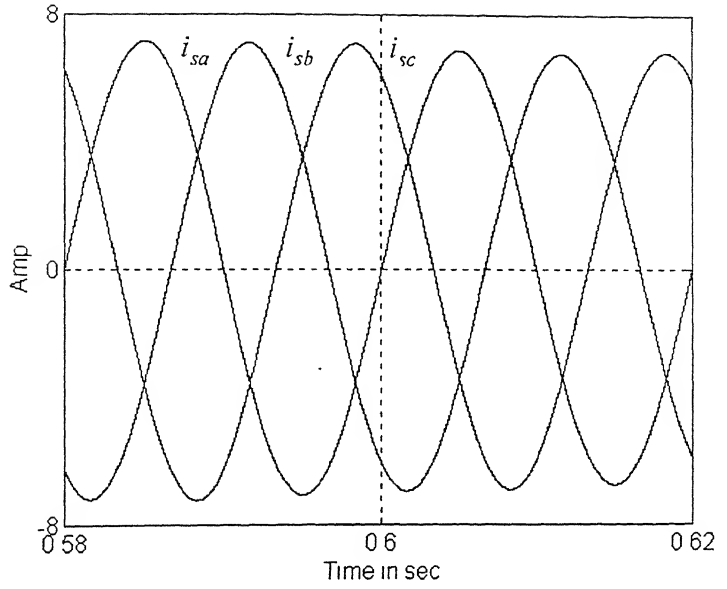


Fig. 2.26 Three-phase reference currents of the source for 30^{th} and 31^{st} cycle with PI controller

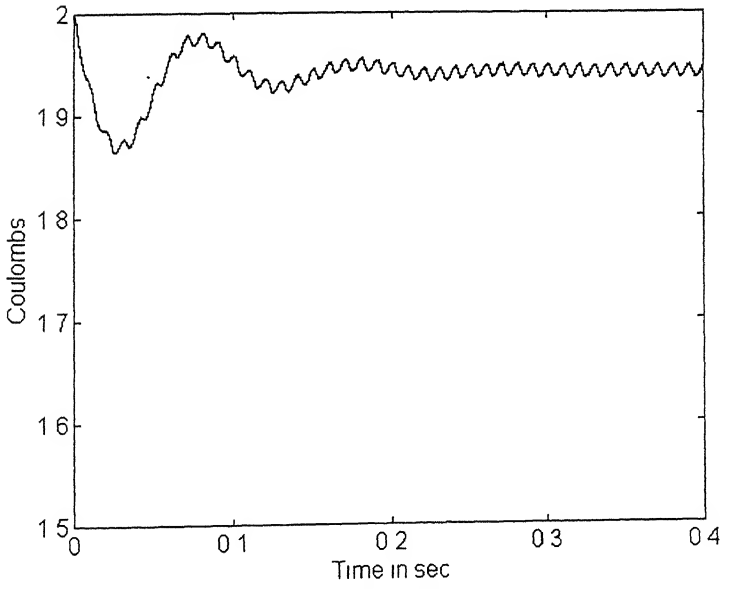


Fig. 2.27 Total charge on capacitors under unbalanced load condition with PD controller

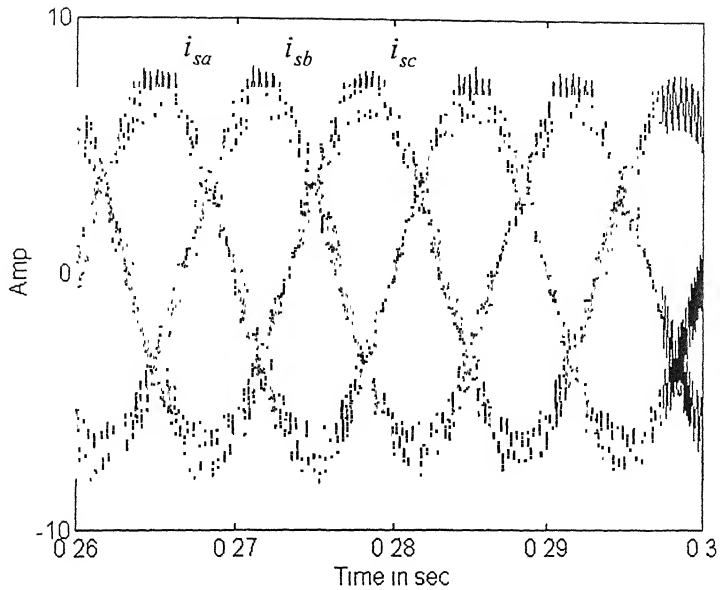


Fig. 2.28 Compensated three phase source currents with PD controller

2.5 CONCLUSIONS

An active harmonic current compensator employing a three-level inverter is investigated. The study reveals that the AHCC is capable of reducing the harmonics created by non-linear loads to a great extent. In this AHCC the fundamental component of load current is extracted using proposed closed loop model and PD controller. The PD controller seems to offer overall excellent performance under all operating conditions. The closed-loop model facilitates control design of the AHCC through frequency response characteristics to achieve different control objectives. This control law takes care of voltage control loop. The extensive simulation studies reveal excellent performance of the AHCC in terms of reactive power compensation, power factor correction, harmonic compensation and load balancing. However as the study reveals, for proper compensation the inverter has to be switched at a high frequency. At a lower switching frequency tracking performance degrades and hence compensation becomes poor. However this being a hard-switched inverter, the switching loss would increase considerably at high frequencies. Therefore usually a compromise is reached between operating power level and inverter switching frequency. Because of the neutral point clamping the three phases are decoupled, therefore this compensator performs much better compared to a

two-level inverter based AHCC. However under extremely unbalanced load conditions the performance of the compensator degrades Additionally this it is difficult to balance the two-capacitor voltages exactly, which might generate unwanted harmonics.

It has been shown that compensator along with simple controller model proposed here has very fast time response and performs well both under balanced and unbalanced load conditions. against all the above mentioned problems. However, the question arises, can a high power hard-switched inverter operate at such a high frequency? It is well known that soft-switched inverters have considerably lower losses than hard-switched inverters. Therefore, they are better candidates for high power AHCC application. In the next chapter we discuss soft-switched inverter based AHCC.

CHAPTER 3

THREE PHASE ACTIVE HARMONIC CURRENT COMPENSATOR USING SOFT-SWITCHED INVERTER

The extensive use of non-linear loads results in harmonic pollution in a power distribution system. There have been efforts from various quarters to mitigate these load current harmonics which otherwise would be drawn from the supply. A number of techniques such as use of passive filters [11], active filtering [14,18,20], hybrid filtering [4] etc. have been suggested in the literature for compensation of line current harmonics. However, all these schemes suffer from one or more drawbacks.

The current regulated PWM shunt compensator has gained prominence as AHCC. However, this compensator has its inherent limitations of high switching losses because of hard switching. This puts a constraint on the maximum switching frequency. For proper current tracking the approximate current bandwidth is usually the PWM frequency divided by a factor of ten. Therefore, a PWM based compensator fails to track high frequency components particularly at high power level. For example, if the harmonics upto nineteenth are to be considered for a 500 KW converter load, then the compensator should have a power rating of 100 kVA and it must be capable of switching at a frequency of about 9.5 kHz or higher. This is a difficult task given the current state of the art of power semiconductor device technology. Thus for active harmonic current compensation, a high power topology with adequate current regulator bandwidth is necessary.

Keeping in view of the above considerations we present an active harmonic current compensator which uses a resonant dc link inverter (RDCLI) as power circuit. The philosophy of using this soft-switched inverter is to obtain a high current regulator bandwidth for compensating higher as well as lower order harmonics. Compensation is achieved by injecting instantaneous compensating current into the supply lines to cancel the harmonics. This compensator can achieve high efficiency by reducing switching losses.

In this chapter RDCLI topology is reviewed. Current initialization issue for RDCLI is addressed. A novel current initialization scheme for RDCLI is proposed. The performance of this inverter as an AHCC is studied for a three-phase system.

3.1 RDCLI TOPOLOGY

The RDCLI was proposed by Divan [31]. This soft-switched inverter is suitable for high power applications (Upto 500 KVA). It also requires a minimum number of devices, is easy to implement and requires simple control. The schematic diagram of a three-phase parallel resonant dc link inverter, that runs from a dc supply (V_{dc}), is shown in Fig. 3.1. It requires an additional inductor and a capacitor compared to a regular pulse width modulated (PWM) inverter. This inductor-capacitor pair forms the resonant circuit. The resonant circuit is connected between the dc source and the inverter so that the input voltage to the inverter oscillates between zero and slightly greater than twice the dc bus voltage.

Fig. 3.2 shows an approximate equivalent circuit of the RDCLI. Here the resistance R in series with the inductance L represents the resistance of the inductor due to its finite Q-factor. It is assumed that the current i_0 remains constant during a resonant oscillation period. Therefore this current is indicated by the current source I_0. The voltage (v_C) across the capacitor is called the dc link voltage. Using the resonant circuit properties, this voltage goes through zero periodically. The six switches that are connected across the link are switched when the link voltage is zero. The switch (S_0) shown in Fig. 3.2 represents the switch across the link. This switch is required to short

the link for the current i_R to build up. The same can be also achieved by shorting the two switches of the inverter in the any leg.

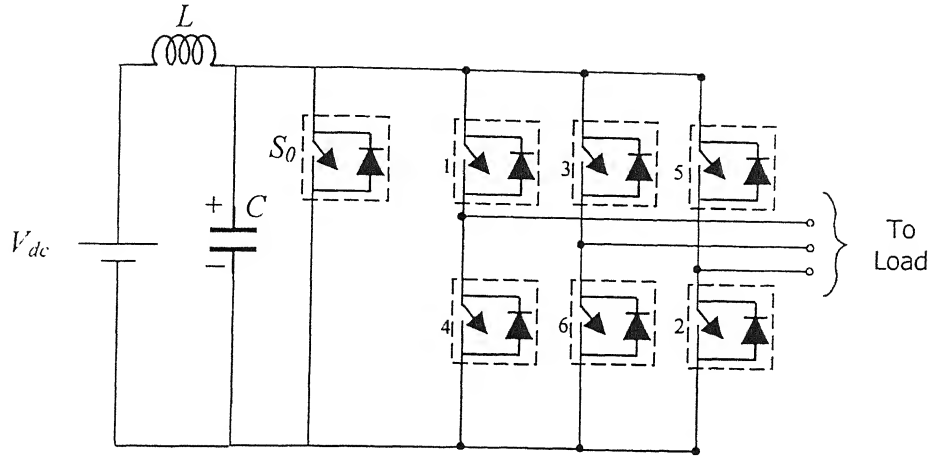


Fig. 3.1 Circuit schematic of a three-phase RDCLI

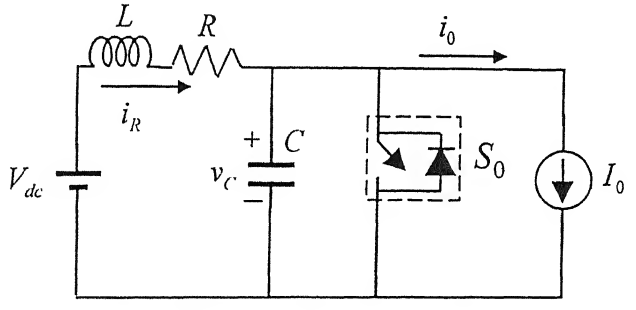


Fig. 3.2 Equivalent circuit of a RDCLI

This simple topology however has few drawbacks — Higher device voltage stresses (especially when the output voltage is greater than twice the dc input voltage) and zero crossing failure unless the initial current in the resonant inductor is built up properly. The voltage overshoot problem can be overcome by using actively clamped RDCLI [32]. It is possible to limit the voltage stresses of the inverter devices to 1.3 to 1.8 times the dc voltage. However, actively clamped RDCLI circuit has few disadvantages [32]. The link frequency varies with variation in the dc link voltage. This shows large current jumps. Furthermore, this topology increases losses due to introduction of the clamping circuit. The additional clamping device increases the complexity of the power and control circuits. Moreover the control of the clamping device becomes extremely

difficult at high frequencies [33]. Therefore, active clamping is not considered in this thesis.

An important consideration for successful operation of RDCLI is that there should not be zero crossing failures, as link voltage (i.e., voltage across the capacitor C) must go to zero at the end of every resonant cycle for zero voltage switching. This is easily achieved if the resonant inductor L has infinite Q factor. In such a case the circuit will oscillate between zero and $2V_{dc}$ with a frequency of $1/2\pi\sqrt{LC}$ Hz. However, in practice an inductor with infinite Q cannot be obtained. Even high quality inductors will have a Q factor around 150 to 200. It is thus important to devise a mechanism through which the dc link voltage is forced to zero at the end of every resonant cycle. This is achieved through the shorting switch S_0. This switch is shorted for a finite duration of time at the end of each resonant cycle to build up the current i_R to a level such that it can overcome the loss (I^2R loss) of the inductor. This will ensure that the voltage will build upto $2V_{dc}$ before becoming zero at the end of the resonant cycle.

This building up of the current to a desired value is called current initialization. It is also to be noted that the inverter switches $(S_1 - S_6)$ are operated through a desired modulation technique only during the interval when the link voltage is maintained zero, i.e., when the shorting switch S_0 is closed. The building up of fixed initial inductor current was first proposed in [31]. However, the initial current is a function of the inverter load current i_0. In a practical circuit, the load current would fluctuate and can also be bi-directional. Thus using a fixed initial inductor current concept would not ensure zero crossing in every resonant cycle unless this current is designed on the worst case basis. Furthermore, this approach would aggravate the voltage overshoot problem. A programmable initial current control technique for an RDCLI was reported in [34]. This scheme is somewhat complex from the implementation viewpoint. In this thesis we present a novel current initialization technique for the resonant circuit which ensures reliable zero voltage switching. The proposed method is based on state transition equation and is simple to implement.

3.2 PROPOSED CURRENT INTIALIZATION SCHEME

The proposed current initialization scheme is explained with the help of waveform of capacitor voltage v_C and link current i_R as shown in Fig. 3.3. The resonant cycle starts at time t_0 and ends at time t_1. Similarly, the next resonant cycle starts at t_2 and ends at t_3. To ensure that no zero-crossing failure occurs at t_3, the current through the inductor L must be built up to the required value. The choice of the interval $t_2 - t_1$ depends on this requirement which, in turn, depends on the output current i_0 and the input dc voltage V_{dc} of the inverter. The instant t_2 is so chosen that the current at this instant is sufficient to bring the capacitor voltage zero again after a resonant cycle.

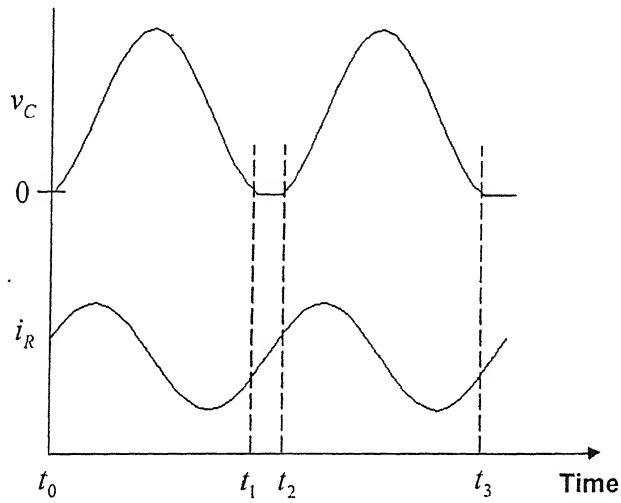


Fig. 3.3 Link voltage and link current waveform

In this thesis we propose a scheme in which the duration $t_3 - t_2$ is fixed at ΔT microseconds. Here, the initial inductor current is generated by shorting S_0 in Fig. 3.2, and a resonant cycle commences with proper values of capacitor voltage (zero) and inductor current. Thus the link capacitor voltage would return to zero after the pre-specified resonant oscillation period ΔT. Fig. 3.4 shows the state-plane trajectory where the transition along the curve (e.g., t_0 to t_1) takes the fixed pre-specified time. The transition along the vertical axis ($v_C \cong 0$) takes a variable time (e.g., t_1 to t_2) depending

on the load current. It is to be noted that the particular value of ΔT chosen depends on the parameters of the resonant circuit. Since a resonant cycle time is much smaller than the time constant of the load circuit, the load current is assumed to be a constant current equal to I_0 over a particular resonant cycle, i.e., between $\Delta T = t_3 - t_2$.

Referring to Fig. 3.2, let us define a state vector as $x = [v_c \quad i_R]^T$ and an input vector as $u = [I_0 \quad V_{dc}]^T$. The state space equation of the circuit is then given by

$$\dot{x} = Ax + Bu \tag{3.1}$$

where the matrices A and B are given by

$$A = \begin{bmatrix} 0 & 1/C \\ -1/L & -R/L \end{bmatrix}, \qquad B = \begin{bmatrix} -1/C & 0 \\ 0 & 1/L \end{bmatrix}.$$

The solution of (3.1) at instant t_3 based on the initial condition at instant t_2 is given by

$$x(t_3) = e^{A\Delta T} x(t_0) + \int_0^{\Delta T} e^{A(\Delta T - \tau)} Bu(\tau) d\tau \tag{3.2}$$

It is to be noted that in the above equation V_{dc} is constant and I_0 is assumed to be known and constant. Also noting that capacitor voltage must be equal to zero at instant t_3, defining a row vector C as $C = [1 \quad 0]$, we can write from (3.2)

$$0 = C[\phi x(t_2) + \theta u(t_2)] \tag{3.3}$$

where $\phi = e^{A\Delta T}$ and $\theta = \int_0^{\Delta T} e^{A(\Delta T - \tau)} B d\tau$. Note that since A, B and ΔT are known a priori, the matrices ϕ and θ can be numerically evaluated. The state plane trajectory

under this boundary value problem is shown Fig. 3.4 where v_C is assumed to be approximately zero when S_0 is closed.

We can expand equation (3.3) as

$$0 = [\phi_{11} \quad \phi_{12}]x(t_2) + [\theta_{11} \quad \theta_{12}]u(t_2)$$

where the subscripts 11 and 12 indicate the particular elements of these matrices. Again from Fig. 3.3 we get $x^T(t_2) = [0 \quad i_R(t_2)]$. Substituting in the above equation and rearranging we get

$$i_R(t_2) = -\frac{1}{\phi_{21}}[\theta_{11}I_0 + \theta_{21}V_{dc}] \tag{3.4}$$

The above value of current at instant t_2 required to ensure zero crossing of the voltage at instant t_3.

Once $i_R(t_2)$ is obtained, there are two ways of obtaining the time for which the capacitor should be shorted. These are discussed below.

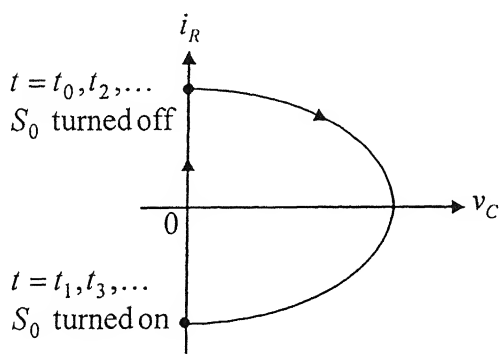


Fig. 3.4 State plane diagram of link voltage and current

3.2.1 Method-1

This is based on mathematical calculation and will produce fairly accurate results. This however is only suitable for simulation studies. The circuit equation for the time interval between t_1 and t_2 is given by

$$\frac{di_R}{dt} = -\frac{R}{L}i + \frac{1}{L}V_{dc} \tag{3.5}$$

The solution of the equation is given by

$$i_R(t_2) = e^{-(R/L)\Delta t} i_R(t_1) + \int_0^{\Delta t} e^{-(R/L)(\Delta t - \tau)} V_{dc} d\tau \tag{3.6}$$

where $\Delta t = t_2 - t_1$. Equation (3.6) is solved to obtain an expression for Δt as

$$\Delta t = \frac{L}{R} \ln\left\{\frac{i_R(t_1) - V_{dc}/R}{i_R(t_0) - V_{dc}/R}\right\} \tag{3.7}$$

There are a couple of problems associated with the above-mentioned approach. The measurement of $i_R(t_1)$ is required for the computation of Δt and this can be available at a time after t_1. This leaves very little time for computation of Δt. It is to be noted that Δt is of the order of a few microseconds. Hence it is almost impossible to compute equation (3.7) in real-time. Even if we assume that this time duration is computed earlier with a prior knowledge of $i_R(t_1)$, it is difficult to generate this time delay using a real-time clock. For example, in one instant this time is computed as 4.71 μs and the next instant it is computed as 4.73 μs. A very high-speed and stable clock and counter circuits will be required to differentiate between these two values in the real-time. Even if the time delay is created using software, this resolution is rather difficult to achieve even with modern high-speed computers.

3.2.2 Method-2

A more practicable solution is to compare the computed value of current $i_R(t_2)$, obtained from equation (3.4), with the actual value link current i_R. The switch S_0 is

As soon as the required initial current is computed in the PC, it is converted into an analogue signal through a DAC. The computation time required is much smaller than the resonant cycle time ΔT. This signal is then available to the comparator for comparison with the actual link current. The link current is monitored continuously through a Hall-effect current sensor. When the link current becomes equal to the required initial current, the comparator output becomes zero and the shorting switch is opened. The monostable is set for giving a pulsewidth of ΔT (oscillation period) after which the switch is shorted. The time for which the link will be shorted will depend on the DAC pre-computed value and the actual current build up. Further details will be discussed in Chapter 6. When the link is shorted, the switching transition of switches $S_1 - S_6$ take place and ZVS is achieved.

3.3 AHCC BASED ON RDCLI

An active harmonic current compensator based on Resonant DC Link Inverter (RDCLI) for three-phase system supplying non-linear loads is investigated. This compensator is connected in parallel with any other non-linear load through filter inductance L_F. Compensation of the line harmonics is achieved by injecting compensating currents into the supply lines such that the compensated line currents are in phase with, and of the same shape as the input voltage. The compensator is controlled by zero-hysteresis bang-bang controller.

The block diagram of the compensating scheme is the same as that of Fig. 2.3 except that the power circuit of the AHCC in this case is implemented by an RDCLI. In the absence of a compensator, the source currents are nonsinusoidal, comprising of fundamental and harmonics that might affect the other loads connected to the same ac bus. If the harmonic components are compensated, then the source currents become sinusoidal. The compensation is achieved on the basis of instantaneous current injection.

In this chapter the performance of the RDCLI as an AHCC is evaluated. The voltage control loop for energy storing capacitor and extraction of compensating currents for the inverter etc. are not addressed. The inverter is energized by a dc source or battery. A typical non-linear load current is simulated. Under perfect compensation condition, the

ac supply source should supply only the active fundamental component of the load current and the compensator should supply the reactive and harmonic components of load current.

It is to be noted that the capacitor voltage control loop is not considered here and hence the fundamental of the load current to be supplied by the source is known a priori. Since this current is known, the compensator reference current can be extracted following the same procedure as discussed in Chapter 2 (eq. 2.2).

As mentioned above, the basic philosophy of an AHCC is to generate a nonsinusoidal current following a command. The RDCLI based AHCC control comprises of two parts. These are

- Choosing a proper value of initial current to avoid zero crossing failure in RDCLI
- Current tracking.

These are discussed below.

3.3.1 Current Initialization

The inverter load current i_0 is calculated in every resonant cycle. This depends on the status of the switches. Assuming that i_0 remains constant at I_0 during a resonant cycle, we can write

$$i_0 = S_{wa}.i_a + S_{wb}i_b + S_{wc}.i_c \tag{3.8}$$

where i_a, i_b and i_c are the phase currents in phases a, b and c respectively. The status of S_{wa} is 1 when the top switch (S_1) in the inverter leg of phase a is on and is zero when the bottom switch (S_4) is on. The same holds for other two phases. Once this current is computed, the required initial current for successful operation of the link can be obtained using the method already described.

3.3.2 Zero Hysteresis Current Regulator

A zero-hysteresis bang-bang control is used for current control of the inverter. However, the switching strategy in this case is somewhat different from a hard-switched PWM current regulated inverter as the switchings in this case can only be done when the link voltage is zero. Therefore instantaneous operation of appropriate switches when the

error crosses the hysteresis band is precluded here. It is needless to mention that three inverter current references are generated for three phases. Just before the zero voltage condition occurs, these three reference currents are compared with their corresponding actual values to generate these error signals. Depending on the polarity of these signals a switching decision is taken. For example, if the error signal of phase-a is positive, then the current through this phase has to be increased. This is done by turning on S_1 and simultaneously turning off switch S_4. Similar switches in other phases are turned on or off depending on their requirements. Since there is no notion of hysteresis band in this case, we will call this as zero-hysteresis bang-bang current control.

3.4 SIMULAION RESULTS

In this section we present the following three tests.

- Frequency response test
- Compensating a three-phase balanced non-linear load
- Compensating a three-phase unbalanced load

The resonant circuit parameters chosen for the study are

- Resonant Circuit: V_{dc}= 700 V, R =0.0531 Ω, L=63.32 μH, C =1μF.
- Interfacing Circuit AC Supply: v_s=440 $\sqrt{\frac{2}{3}}$ sin (100πt).

3. 4. 1 Frequency Response Test

A RDCLI is normally used for motor drive applications. However, we intend to use it for active filtering [24]. It is thus imperative that the inverter should be able to track high frequency signal.

The purpose of the frequency response test is to demonstrate the high current regulator bandwidth of the inverter. In this test the inverter is constrained to follow a reference current in a zero-hysteresis bang-bang current control mode by properly gating the switches. The inverter is subjected to follow two high frequency sinusoidal components of 650 Hz and 1350 Hz. Fig. 3.6 shows the above mentioned reference current waveform and its tracking. It is clear from this figure that the inverter is capable of tracking these high frequency components. The tracking is accurate. However, this current contains some high frequency ripple as seen from this figure.

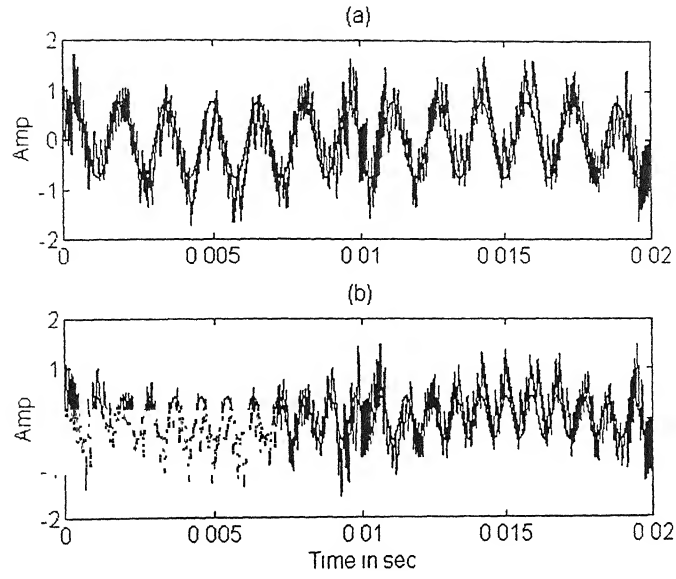


Fig. 3.6 Frequency response of the inverter

3. 4. 2 Non-Linear Load Compensation

The viability of the AHCC is tested through this simulation. The interfacing circuit parameters are: L_F =15 mH, R_F = 0.2256 Ω. It is assumed that ac supply system frequency is 50 Hz and the peak line to line voltage magnitude is 440 Volts. The ac side of the inverter is connected to the supply through interface circuit. Fig. 3.7 shows the simulated load current. The load current contains 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd} and 25^{th} harmonics other than the fundamental component. Fig. 3.8 shows the inverter reference current and its tracking. Under this situation the compensated currents from the source are shown in Fig. 3.9. From these figures it is clear that the tracking is not quite proper and it particularly fails to track the fast rising edges of the reference current.

The rate of rise of compensating current depends on interface inductance and the dc source voltage. This is explained below. The instantaneous compensator current is governed by the following equation.

$$L_F \frac{di_F}{dt} = V_{lnk} S - v_S \sin \omega t \tag{3.9}$$

where V_{link} is the voltage across the dc link. The instantaneous inverter phase voltage will depend on link voltage V_{link} and its associated switching function S. From the above equation we can write

$$\frac{di_F}{dt} = \frac{\Delta V}{L_F} \tag{3.10}$$

Therefore the rate of rise of current through this inductance can be increased if ΔV increases. The source voltage being a constant, this quantity can be raised if the inverter phase voltage can be increased. Thus a higher value of V_{dc} will raise the link voltage, and therefore will be able to force the required compensator current. With all other parameters remaining same, the dc source voltage is increased to 1000 Volts. The inverter current reference and its tracking are shown in Fig. 3.10 and compensated source currents are shown in Fig. 3.11. As seen from the result compensation is still not perfect, while two current waveforms are in proper shape the third one is improper. This is the result of unconnected neutral. We further investigate this effect with the following test.

3. 4. 3 Load Balancing

A much worse load is now considered in which the AHCC has to do harmonic suppression and load balancing. The load is severely unbalanced with two phase carrying 10 A (peak) current while the third phase is open (i.e., zero current). These currents carry harmonics upto 25^{th} order. The two non-zero load currents are shown in Fig. 3.12 (a-b). The phase difference between these currents is maintained at 120°. The compensated source currents are shown in Fig. 3.13. The currents are completely unbalanced even after compensation. This is explained below.

As opposed to a three-level inverter, in a three-phase RDCLI there is no path for neutral currents. Therefore the current in each phase will depend not only on the switching state of the corresponding inverter leg, but also on the state of other two inverter legs [45]. This will force the current regulator to experience interaction between the phases.

The situation even worsens for an unbalanced load condition. The three-phase inverter in this case is required to act as an AHCC where its job is not only harmonic

compensation but also load balancing. This implies that the AHCC must supply currents in such a way that the source sees balanced currents. This in turn means that the references that are obtained for the compensator are also unbalanced. However, the sum of the three-phase currents of the inverter has to be zero as there is no neutral path. Therefore this unbalance will be present in the actual compensator currents. This will also be reflected in the source currents. This is shown in Fig. 3.13.

However, if the inverter is not constrained to supply these unbalanced currents, then the situation will be different. Let us assume that we use the compensator for the first two phases only. The compensator reference for the 3rd phase is forced such that the sum of the three currents is zero. The compensated source currents under this condition are shown in Fig. 3.14. The phases 'a' and 'b' are properly compensated while the third phase sees an arbitrary waveform. This is neither desirable nor expected. We must therefore abandon the idea of using the three-phase RDCLI as an AHCC.

Just not RDCLI, this will happen in any topology with an unconnected neutral. Therefore, with the commonly available RDCLI topology, it is difficult to achieve perfect compensation.

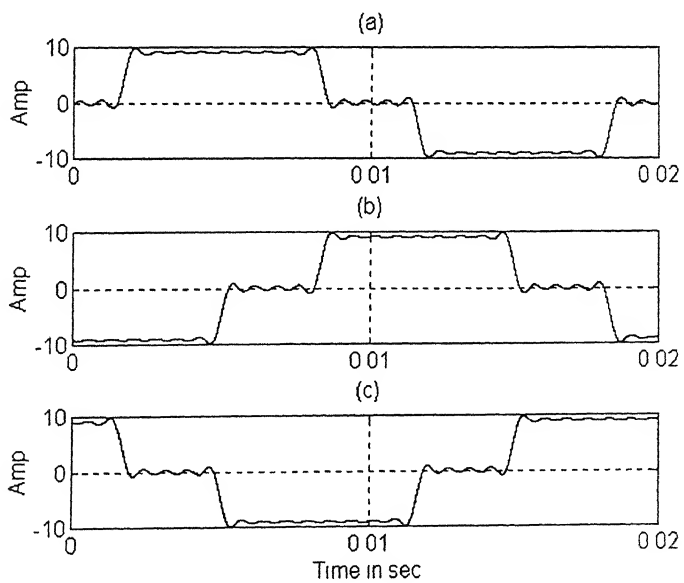


Fig. 3.7 Simulated load current for phases 'a', 'b' and 'c' are shown in (a), (b) and (c) respectively

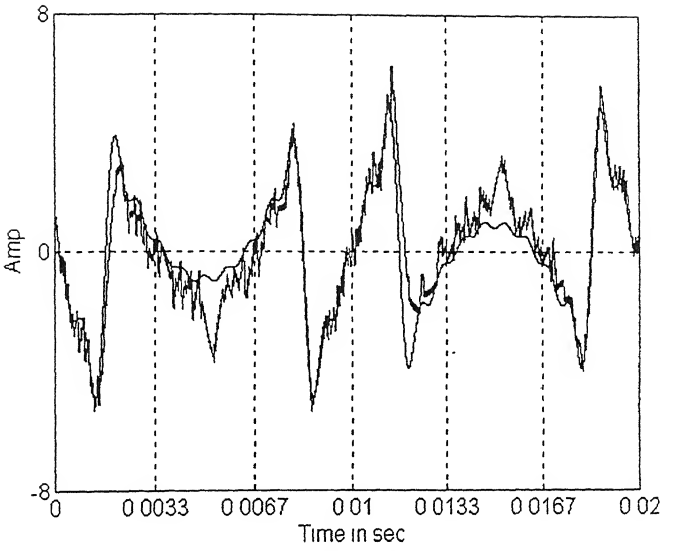


Fig. 3.8 Inverter reference current and its tracking

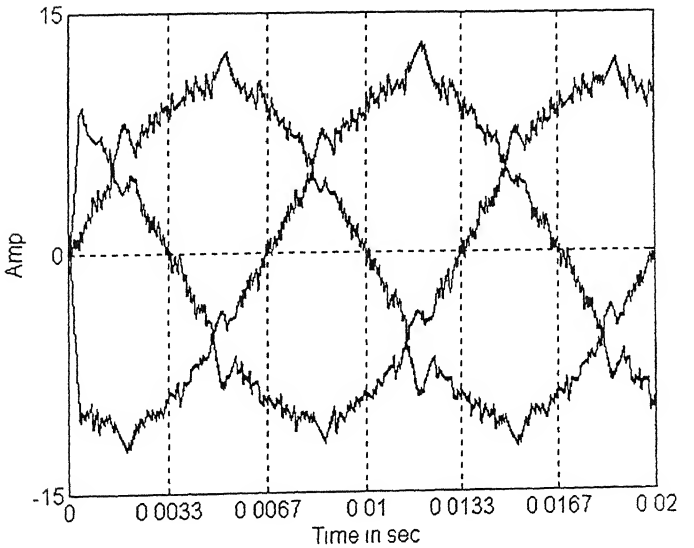


Fig. 3.9 Source currents after compensation at V_{dc}= 700 Volts

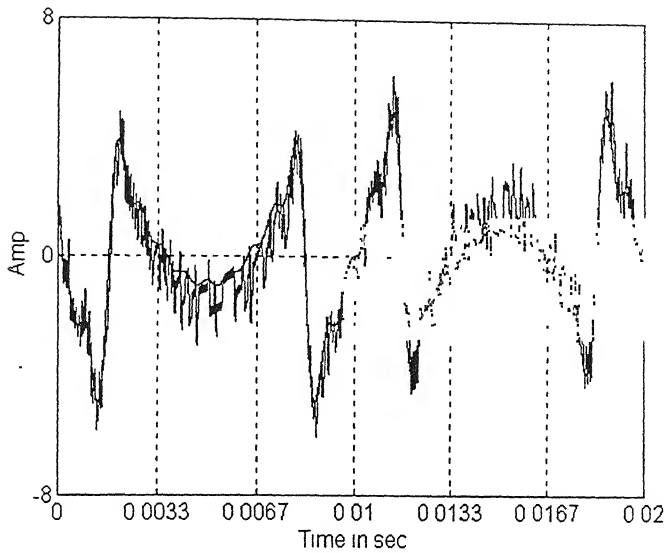


Fig. 3.10 Inverter reference and output current for phase 'a' at V_{dc}= 1000 Volts

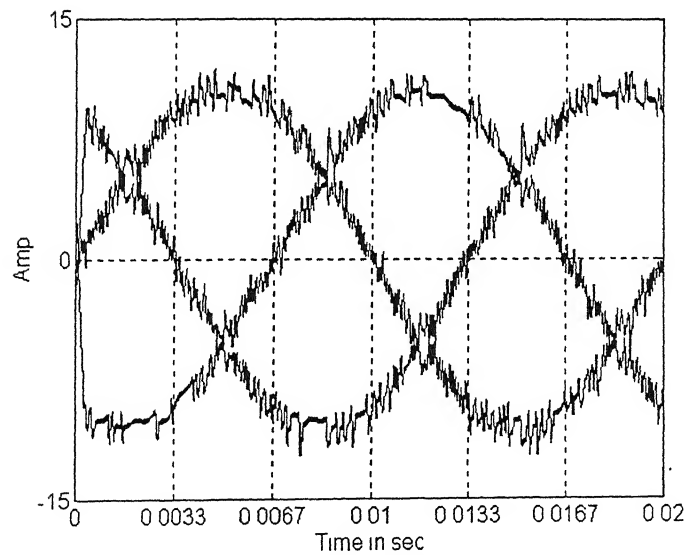


Fig.3.11 Compensated source currents at V_{dc}= 1000 Volts

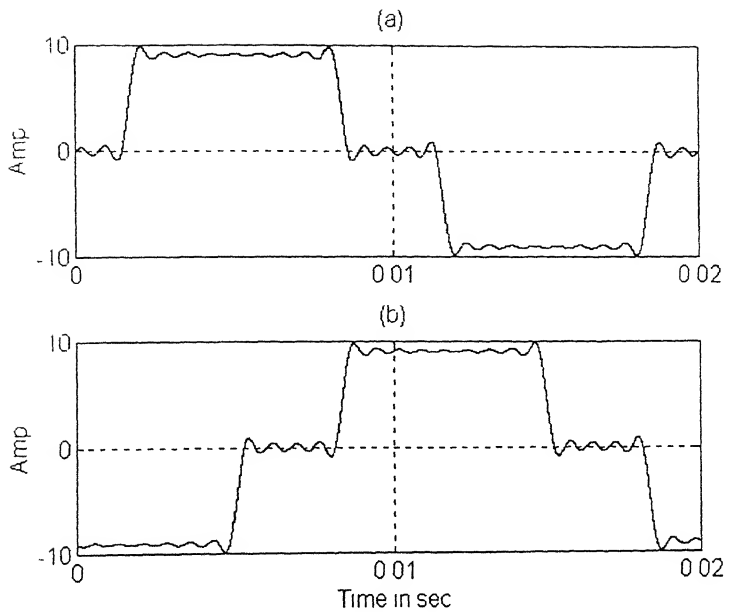


Fig. 3.12 Simulated load currents under unbalanced condition

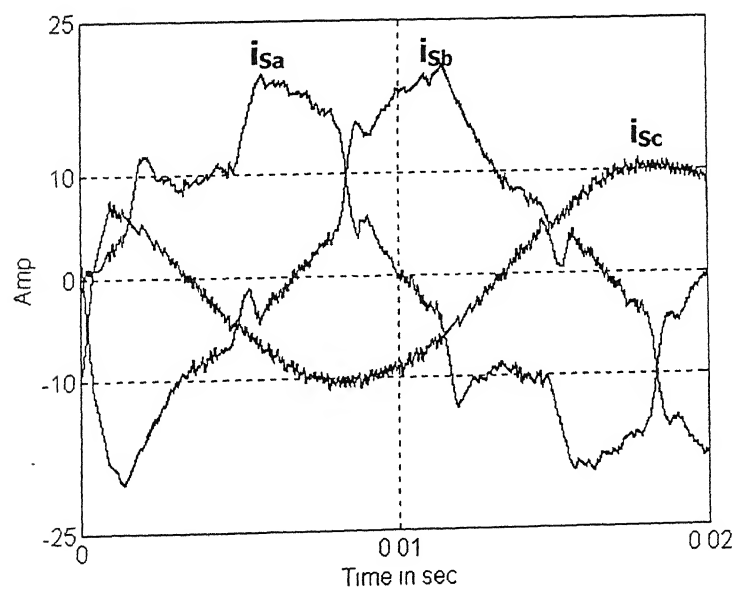


Fig. 3.13 The three-phase source currents after compensation

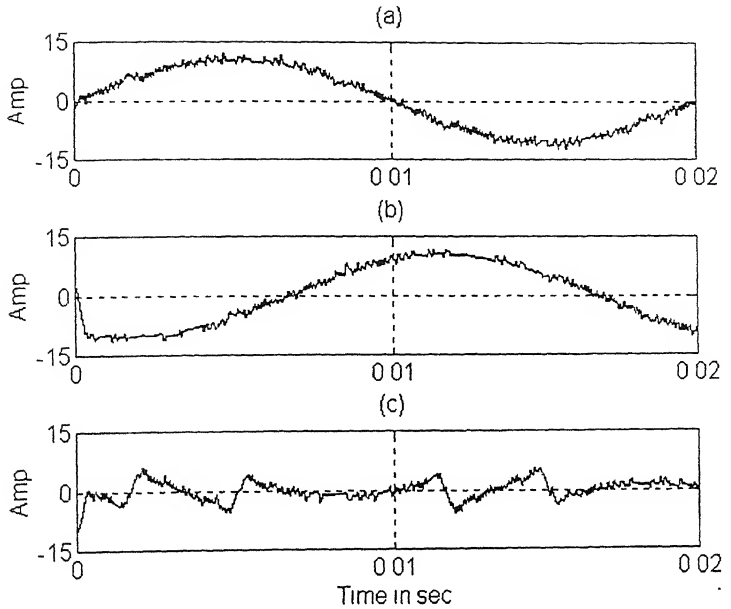


Fig. 3.14 Currents in three phases are shown in (a), (b) and (c).

3.5 CONCLUSIONS

A new current initialization scheme for resonant dc link inverter is proposed in this chapter. This initialization scheme is based on boundary value problem. It is shown that that this current can be predicted very accurately which in turn ensures the zero-crossing of the link voltage at a prescribed time instant. The proposed scheme is validated through simulation studies. An active harmonic current compensator using RDCLI as power circuit is investigated. This soft-switched inverter based AHCC is capable of canceling the load current harmonics reasonably. However, it is observed that its performance is acceptable only for balanced systems. It is seen that usually while tracking in two phases is accurate, there seems to be minor errors in the third phase. The performance completely deteriorates in case of unbalanced loads. These errors are the effect of unconnected neutral. Therefore for greater flexibility single-phase AHCC is considered next.

CHAPTER 4

SINGLE PHASE AHCC USING HARD-SWITCHED PWM INVERTER

The concept of active harmonic current compensation is discussed in the earlier chapters. The problems associated with three-phase AHCC are already presented in Chapters 2 and 3. For greater flexibility and better performance under unbalanced load conditions, single phase AHCC is considered in this chapter. In the present study we consider single-phase hard-switched PWM inverters as the power circuit. This inverter is typically operated in a current regulated PWM mode to synthesize currents that are antiphase with the supply harmonics. Summing these currents at the point of common coupling causes the harmonics to cancel. As a result clean sinusoidal in phase current flows from the source and filtering is achieved. The results are validated through digital computer simulation studies in which two different controllers are used.

4.1 PRINCIPLE OF AHCC

The schematic diagram of the AHCC is same as that shown in Fig. 2.3. The compensator is controlled in a closed-loop manner. The inverter switches are controlled to actively shape the current through the inductor following a command current such that the input current from the source is in phase and of the same shape as the input sinusoidal voltage.

Two control strategies are suggested in this chapter for extraction of fundamental component of load current. These control strategies take care of voltage control of

energy storing capacitor. The PWM inverter is operated in hysteresis current control mode for shaping the inverter current.

4. 2 EXTRACTION OF COMPENSATOR REFERENCE

In this section we present two different controllers that are used for dc voltage control and reference current extraction.

4.2.1 Method-1

The block diagram of the control scheme is shown in Fig. 4.1, which is very similar to the one shown in Fig. 2.4. This control strategy is already described in Chapter 2 (section 3). Here the same control design is used for a single phase AHCC. We have pointed out in Chapter 2 that the capacitor charge would contain ripples in the presence of harmonics and under unbalanced load conditions. In order to filter out these ripples the error in charge is passed through a low pass filter. However, it was also observed that with a low cut-off frequency of the LPF the settling time of the controller would be large. Therefore in order to obtain a faster response a moving average filter (MAF) is connected at the output of the controller. This filter has a settling time of half a cycle. Additionally, this would smooth out the controller output. The controller output u is passed through the MAF. In a moving average filter, a moving window of fixed time duration is used to find the average value of the input waveform. In this case a time period of half cycle is chosen. The reference waveform for the source current is obtained through the multiplication of k (MAF output) by sin ωt (the template of source voltage). The compensator reference is then obtained in the usual manner. The controller $G_c(s)$ in this case can either be a PI or PD controller. However, we shall concentrate on the PD controller only.

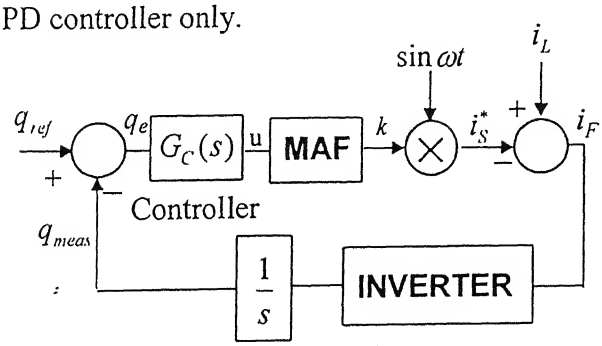


Fig. 4.1 Block diagram of PD controller.

4.2.2 Method 2

The block diagram of the control system is shown in Fig. 4.2. It includes two moving average filters MAF_1 and MAF_2. The time period of both the MAFs are chosen to be half cycle. The instantaneous load real power is filtered every half a cycle through MAF, to extract the average load power P_{Lav}. If the source voltage and current are in phase, the average power is given by

$$P_{Lav} = V_{srms} I_{srms} = \frac{V_{sm} I_{sm}}{2} \tag{4.1}$$

where V_{sm} and I_{sm} are respective peak values of source voltage and source current respectively. From equation (4.1) we get

$$I_{sm} = P_{Lav} \frac{2}{V_{sm}} \tag{4.2}$$

Assuming that V_{sm} is known, we can extract the peak of the source current required to supply the load real power.

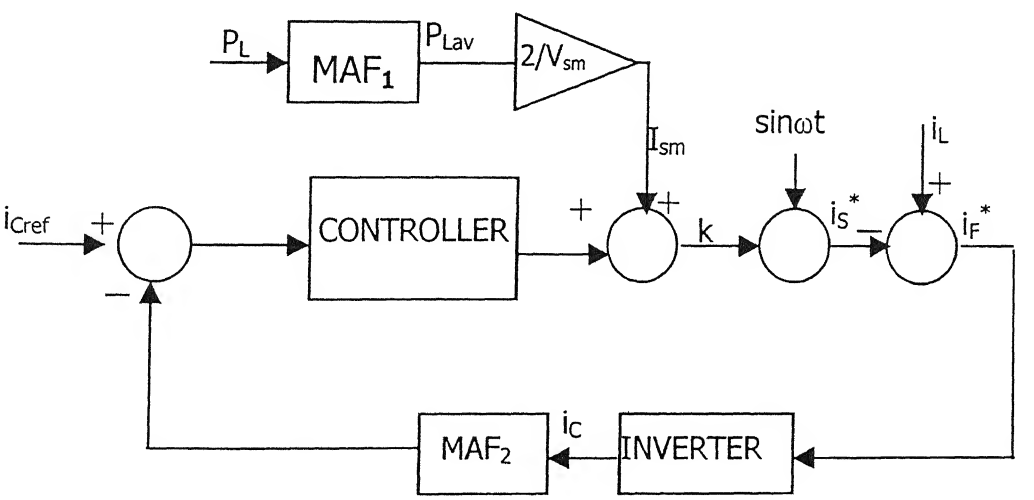


Fig. 4.2 Block diagram of controller—2

As mentioned before, the source must supply the losses in the inverter circuit in addition to the source current. To facilitate this, we consider the current (i_C) flowing through the dc storage capacitor. This current is actually the inverter current multiplied

by the switching function. Now the dc capacitor voltage is governed by the following differential equation

$$C\frac{dv_c}{dt} = i_c \tag{4.3}$$

The solution of the equation between 0 and t_1 is given by

$$v_c = \frac{1}{C}\int_0^{t_1} i_c dt + V_{c0} \tag{4.4}$$

where V_{c0} is the initial value of the capacitor. Assuming that $t_1 = \frac{2\pi}{\omega}$, the capacitor voltage will remain constant at V_{c0} if the average of the capacitor current over one cycle is zero.

From the above consideration, the capacitor current i_C is passed through MAF_2 to find its average over a full cycle. Since the current must be zero, it is compared with zero and the error is given to a controller. The output of the controller is added with I_{sm} to form the peak of the current to be drawn by the source. This way the losses in the inverter circuit are replenished by the source to maintain the dc capacitor voltage.

4.3 SIMULATION RESULTS

The simulation results obtained through MATLAB are presented in this section. The single-phase full-bridge voltage source inverter (VSI) that runs from dc storage capacitor is simulated. The inverter is connected in parallel with non-linear loads through an interface inductor. The data used for the simulation studies are:

- Capacitance of DC storage capacitor: 1000μF.
- AC Supply: System Frequency: 50 Hz, $V_{sm} = 70V$
- Interface Circuit: $L_F = 10mH$ $R_F = 0.2\Omega$

Tests are performed using the two controllers discussed before.

4. 3. 1 Results with Controller—1

The PD controller parameters used are:

$$K_p = 100, K_D = 40, N = 20.$$

The simulated load current is assumed to be non-linear and it contains fundamental component and odd harmonics from 3rd to23rd. The peak value of the fundamental current is 5 A. The magnitude of the harmonic components is inversely proportional to the harmonic number. Fig. 4.3 (a) shows the simulated load current. The inverter is operated in hysteresis current control mode and the hysteresis band is chosen 0.5 A. The compensated source current is shown in Fig. 4.3 (b). This shows that the source current becomes sinusoidal within two cycles (0.04 sec) after the compensator is switched on. This current however contains some high frequency ripple. The other simulation results with this controller are shown in Fig. 4.4 through to Fig. 4.10.

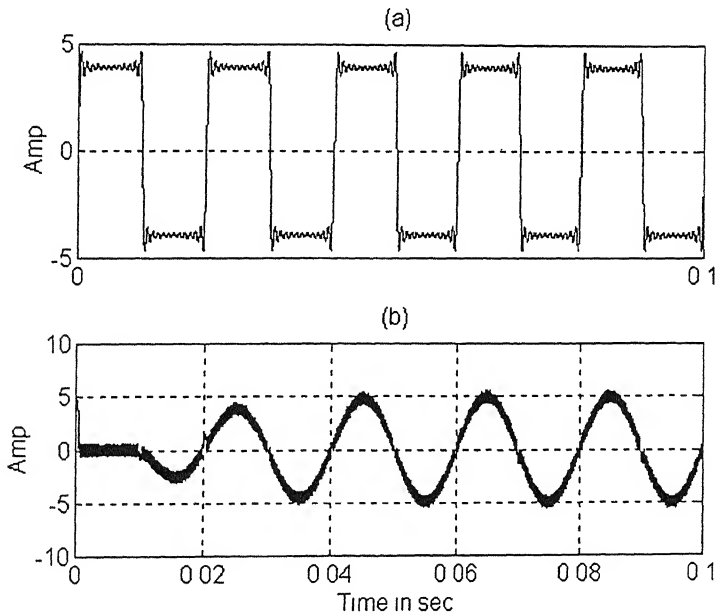


Fig. 4.3 (a) Simulated load current, (b) Source current after compensation

The tracking performance of the inverter is depicted in Fig. 4.4 (a). It is observed that the inverter is effective in following its command current. The same waveform is zoomed for one cycle in Fig, 4.4 (b). The source voltage (scaled down by a factor of

ten) along with compensated source current is shown in Fig. 4.5. It is needless to say that power factor correction is achieved.

The inverter is operated with a hysteresis band of 0.5 A; with this condition the inverter average switching frequency is 5.4 kHz. The magnitude of various individual frequency components for the uncompensated and the compensated system are shown in Fig. 4.6 (a) and (b) respectively. From these figures total harmonic distortion (THD) is obtained. The THD comes down to 3.22 % after compensation from 43.78 % in the uncompensated system. The THD is usually treated as a figure of merit for any compensator and in this regard the compensator can be considered to be ideal.

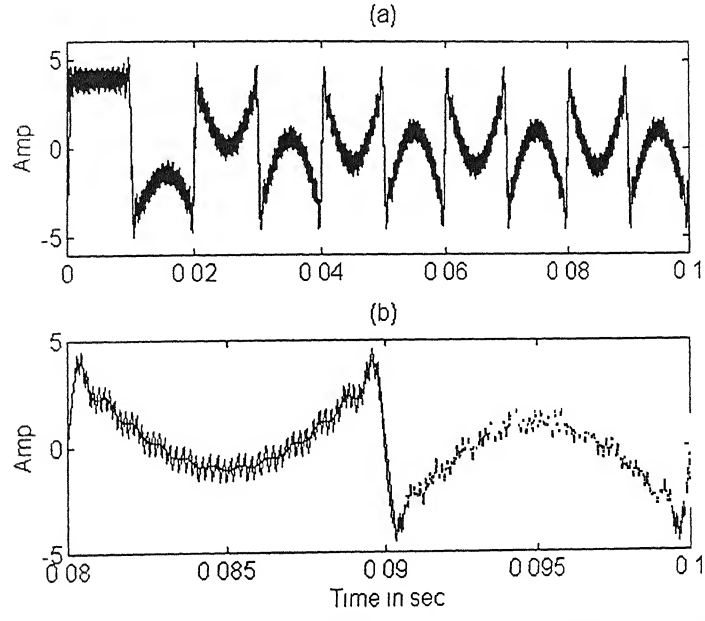


Fig. 4.4 (a) Compensator reference and its tracking, (b) Same waveform as in (a) in an expanded scale

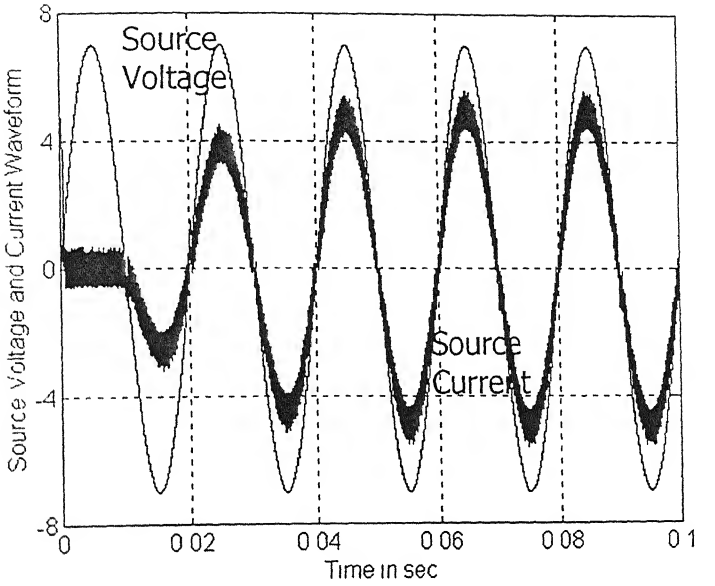


Fig. 4.5 Source voltage (scaled down by a factor of ten) and source current after compensation

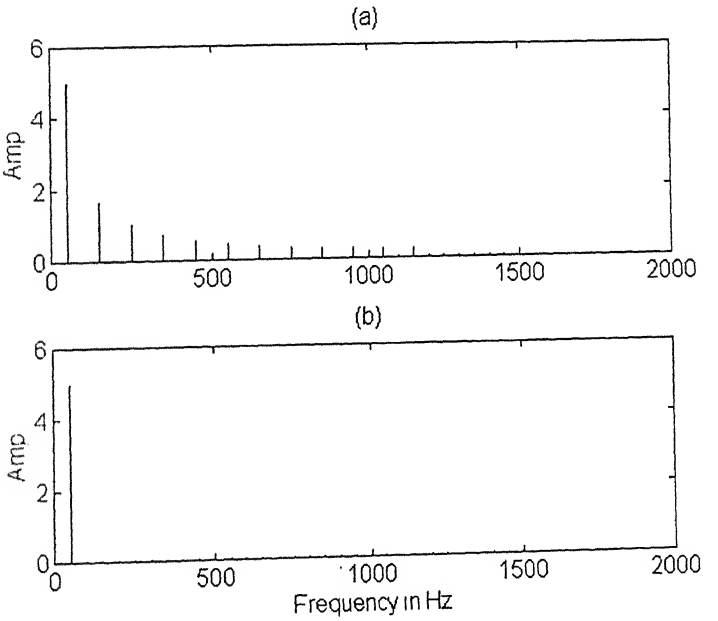


Fig. 4.6 Frequency response (a) Uncompensated system (b) Compensated system

The controller output u for this case is shown in Fig. 4.7 (a). It can be seen that this contains ripple of small magnitude and a frequency that is roughly equals double the fundamental frequency. To eliminate this undesirable effect this signal is passed through an MA filter as shown in Fig. 4.1. The output of the MAF is shown in Fig. 4.7 (b). It can

be seen that this does not contain any ripple. As mentioned earlier, this filter introduces an additional delay of half cycle, which is evident from Fig. 4.7 (b).

Fig. 4.8 shows the capacitor charge waveform. It is clear that the capacitor charge remains essentially constant after the initial transient showing the effectiveness of the controller.

In order to investigate the performance of the compensator at a lower switching frequency, the hysteresis band is increased to 1A. Under the circumstances the switching frequency is 3.2 kHz. The compensated source current is shown in Fig. 4.9 (b). This is shown simultaneously with the compensated source current from previous simulation for switching frequency 5.4 kHz (Fig. 4.9 (b)) for comparison purpose. It is clear that high frequency switching is essential for better tracking purpose. It is also evident that the source current distorts around zero crossing for lower switching frequency. The spectra (i.e., the amplitude of different frequency components) of the compensated source current is shown in Fig. 4.10. The THD under this situation becomes 7.12 %.

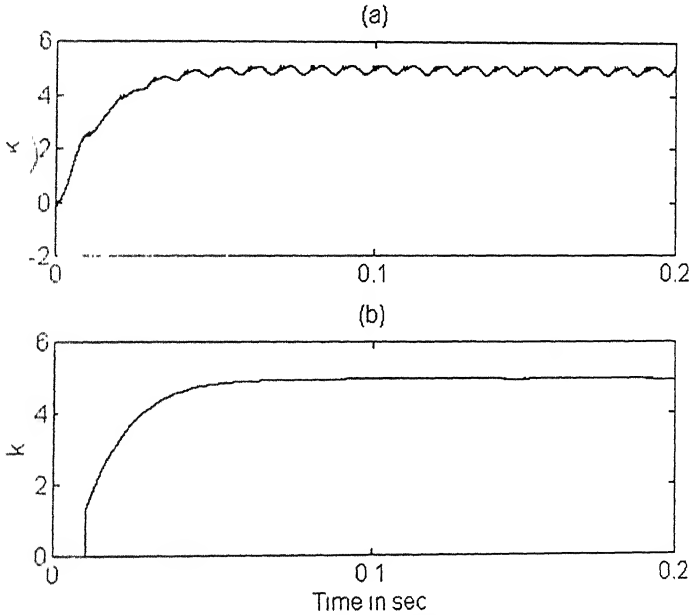


Fig. 4.7 (a) Controller output (b) Output after moving average filter

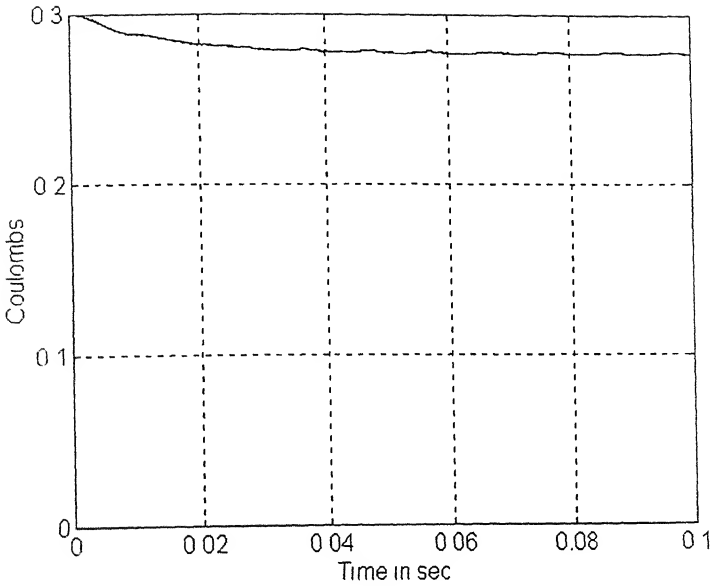


Fig. 4.8 Waveform of DC capacitor charge

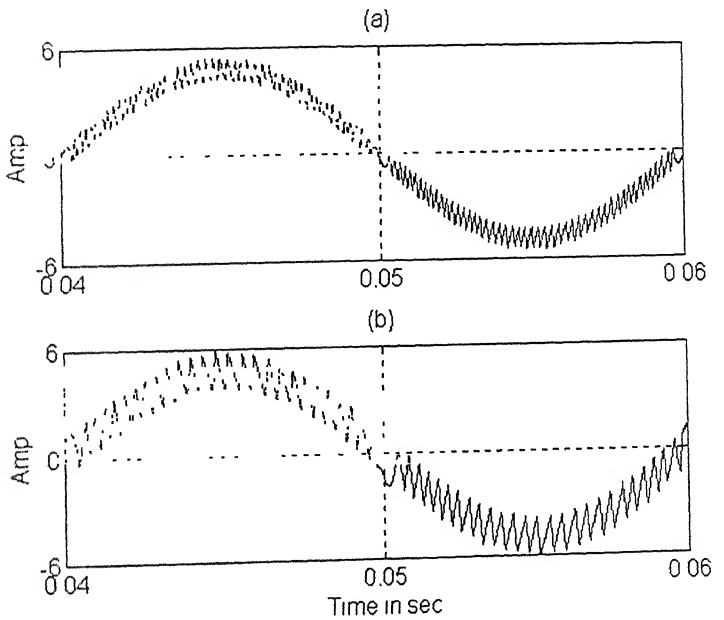


Fig. 4.9 Compensated source current at (a) 5.4 kHz (b) 3.2 kHz

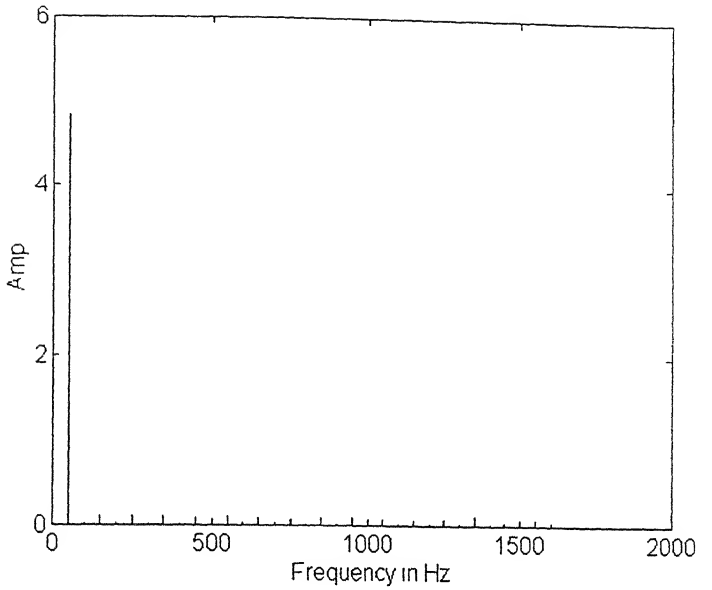


Fig. 4.10 Frequency spectra after compensation for switching frequency 3.2 kHz.

4.3.2 Results with Controller—2

Similar results are also obtained through controller-2. The parameters of the PI controller are:

$$K_p = 5, K_i = 0.005.$$

The same load current is considered as shown in Fig. 4.3 (a). The simulated load current and the compensated source currents are shown in Fig. 4.11 (a) and (b) respectively. The delay in this case is about 4 cycles.

The compensator reference and its tracking are depicted in Fig. 4.12 (a). It is observed that the inverter is effective in following its command current. The same waveform is zoomed for one cycle in Fig, 4.12 (b). The source voltage (scaled down by a factor of ten) along with compensated source current is shown in Fig. 4.13. It is needless to say that power factor correction is achieved.

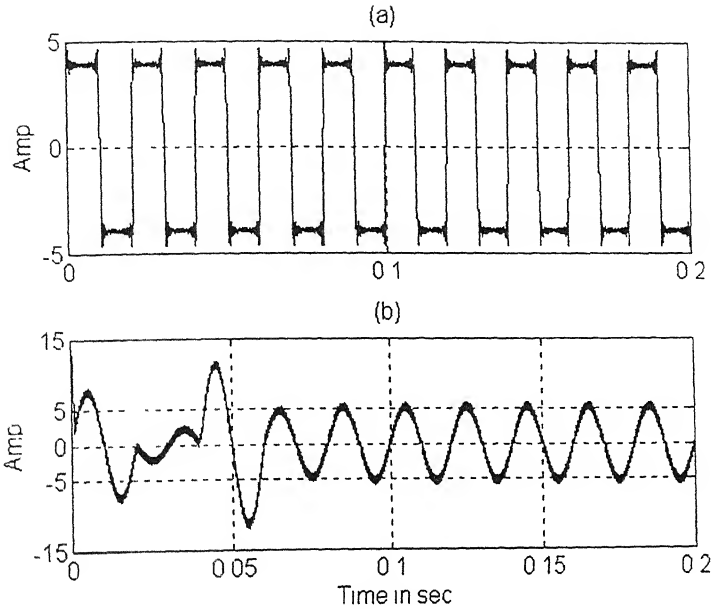


Fig. 4.11 (a) Simulated load current (b) Compensated source current

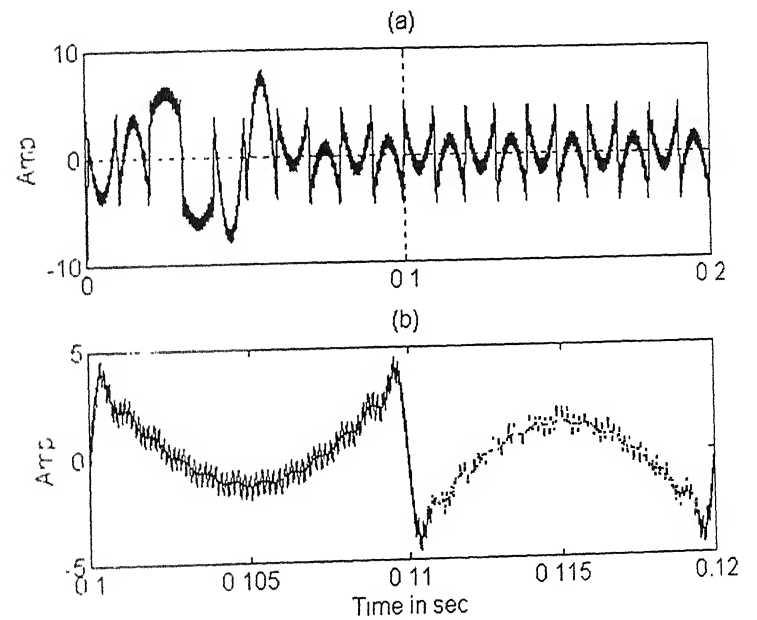


Fig. 4.12 (a) Compensator reference and its tracking, (b) Same waveform as in (a) in an expanded scale

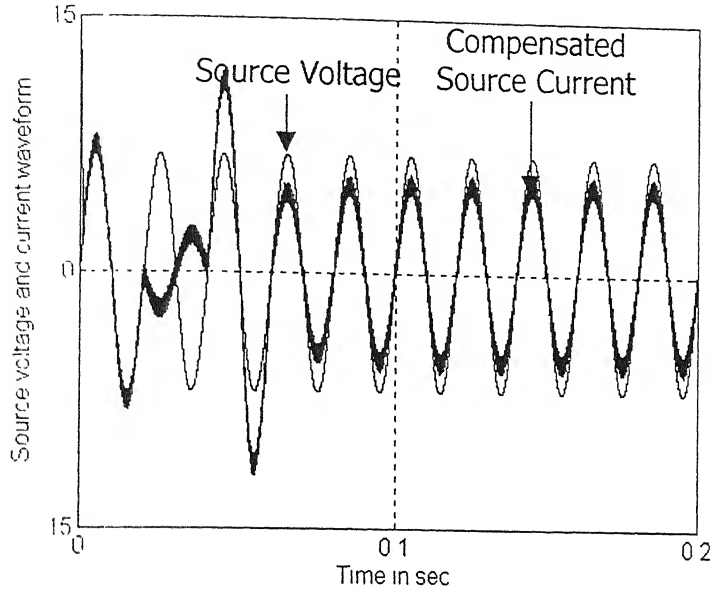


Fig. 4.13. Source voltage (scaled down by a factor of ten) and compensated source current

The amplitudes of different harmonic components of the load current are shown in Fig. 4.14 (a). The same waveform for the compensated source current is shown in Fig. 4.14(b). The THD is found to be 3.72 % after compensation, which is quite good. However, it is seen that with some load conditions, it becomes difficult for maintaining a steady voltage across the dc storage capacitor. This particularly happens when the correction is not proper.

4. 3. 3 Comparison of two Controllers

The performance of the AHCC in conjunction with controller—1 is very good. Compensation is achieved and voltage regulation is obtained. The response is also quite fast. The performance of the AHCC with controller—2 is also satisfactory, however the response is slow when compared to the PD controller.

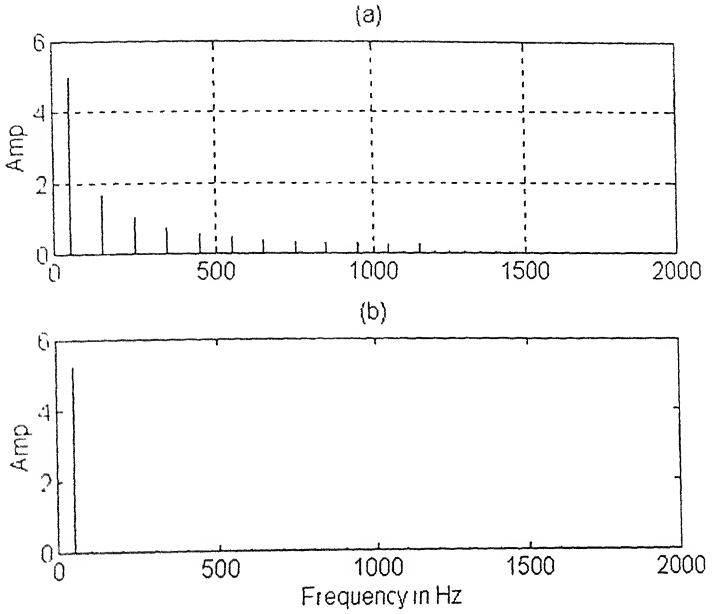


Fig 4.14 Frequency spectra of (a) Uncompensated system (b) Compensated system

4. 4 CONCLUSIONS

The performance of single-phase hard-switched inverter based AHCC is studied. The compensator performance improves with the increase in inverter switching frequency. The proposed PID controller facilitates extraction of the compensator reference effectively.

CHAPTER 5

SINGLE PHASE AHCC USING SOFT-SWITCHED INVERTER

The advantages and limitations of three-phase AHCC are brought out in Chapters 2 and 3. The limitations of hard-switched inverters as power circuit in AHCC application are also brought out in Chapters 2 and 4. We have concluded that for active harmonic current compensation, a high power topology with adequate current regulator bandwidth is necessary. The limitations of three-phase RDCLI based AHCC is already presented. The major problem is due to unconnected neutral. These limitations can be eliminated using a single-phase AHCC. In this chapter we discuss the use of two soft-switched inverters for AHCC application in single-phase versions. The compensation scheme has advantages such as reduced switching loss, fast transient response, adequate current regulator bandwidth and simple control strategy.

5. 1 RDCLI BASED AHCC

The block diagram of the compensating scheme, shown in Fig. 5.1, is similar to the one shown in Fig. 2.3 except that in this case a single-phase ac source is supplying a single-phase non-linear load. The power circuit is a single-phase RDCLI as shown in Fig. 5.2. As explained earlier, in the absence of a compensator, the source current would be non-sinusoidal as dictated by the non-linear load, comprising of fundamental and harmonics, which will affect the other loads connected to the same common coupling point (point p in Fig. 5.1).

First we study the use of RDCLI for AHCC application. The basic purpose of an AHCC is to generate a non-sinusoidal current following the command current. In this

section we only study the performance of single-phase RDCLI topology for AHCC application. The voltage control loop for energy storing capacitor is not considered. Moreover, the load current is assumed to be known a priori. Ideally the source should supply only the active fundamental component of the load current. Therefore for this study we assume compensated source current (i_S) equals fundamental component of load current (i_l).

5.1.1 Control Strategy

The RDCLI based AHCC control comprises of two parts. These are — (1) choosing a proper value of initial current to avoid zero crossing failure in RDCLI and (2) current tracking. These are discussed below.

5.1.2. Current Initialization

The concept and requirement of current initialization is already discussed in Chapter 3 (Section 2). The initial current requirement in the inverter depends on current i_0 (i.e. the load current of resonant link). The value of i_0 can be obtained using $i_0 = S\, i_F$; where S can take value 1, 0, -1 depending on the switching logic.

5.1.3 Current Tracking

A zero-hysteresis bang-bang control is used for current control. This is already described in Chapter 3 (Section 4. 2). As this is a zero voltage switching inverter, the switching transitions take place only at the prescribed instants when the link voltage is zero. Prior to zero crossing, the actual output current of the inverter is compared with the reference current. Based on the error signal, a switching decision is taken such that the inverter output voltage is $S v_{c\cdot}$; where $v_{c\cdot}$ is the link voltage and S may have values 1, 0 or -1 depending on the switching conditions. The inverter is switched such that it facilitates the flow of required current.

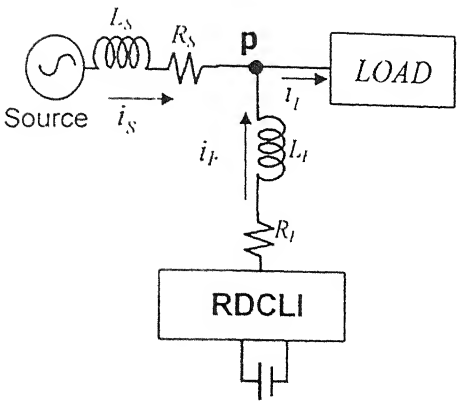


Fig. 5.1 Block schematic of RDCLI based single-phase AHCC

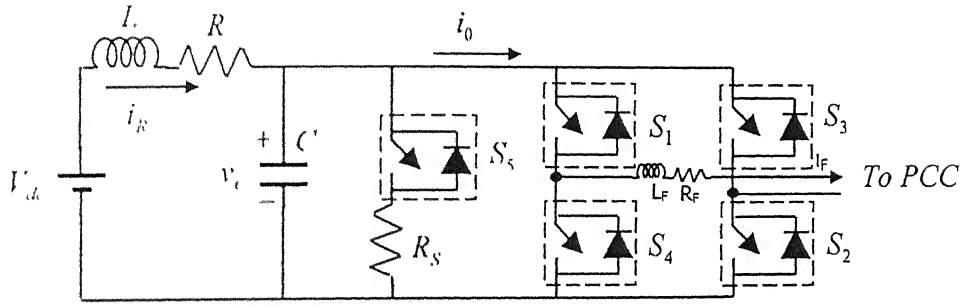


Fig. 5.2 Schematic of single-phase RDCLI as compensator.

5.1.4 Effect of Link Frequency Variation on Compensation

The RDCLI active harmonic current compensator is simulated using the MATLAB software package. First we study the effect of link frequency variation on compensator performance.

The system parameter chosen are:

- Interface Circuit: $L_F = 15$ mH, $R_F = 0.2256\ \Omega$
- AC Supply: $v_s = 440\sqrt{\frac{2}{3}}\sin(100\pi t)$ V
- Resonant Circuit: $R = 0.0531\ \Omega$, $L = 63.32\ \mu$H, $C = 1\ \mu$F, $V_{dc} = 385$ V.

The simulations are carried out at three different link frequencies, 20 kHz, 40 kHz and 80 kHz. The resonant cycle time ΔT (oscillation period as described in Section 3.2) chosen for the above three frequencies are 45μs, 22.5μs, and 11.25μs respectively. It is assumed that the non-linear load draws a current that contains 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 13^{th} and 23^{rd} harmonics in addition to the fundamental. The magnitude of the fundamental component is chosen to be 10 A. The magnitudes of the harmonic components are assumed to be inversely proportional to the harmonic number. This particular choice of the load current is to demonstrate the performance of the AHCC and not based on any particular power-electronic load. The compensated source currents for three different frequencies are shown in Fig. 5.3.

It is seen that even though compensated current becomes smoother with an increase in the link frequency, notches that are visible around the peak of the current waveform in Fig. 5.3 (a), only reduce but are not eliminated with an increase in link frequency. These notches can be reduced significantly by increasing the dc source voltage V_{dc}.

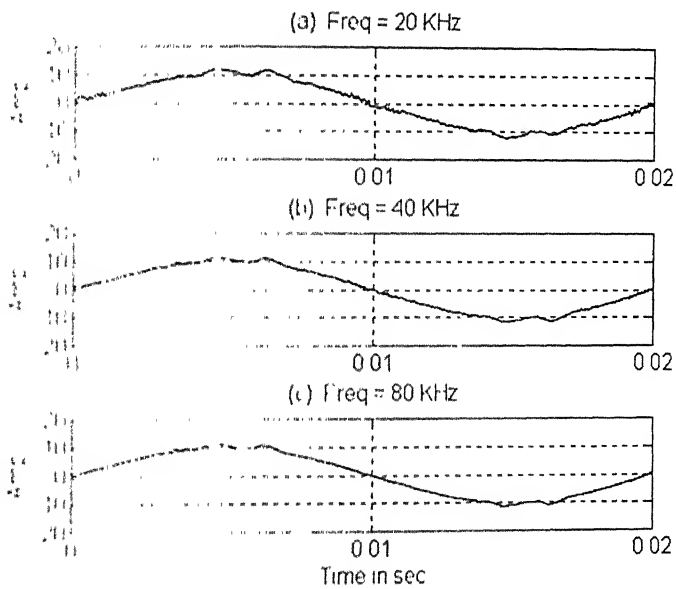


Fig. 5.3 Compensated source currents from source at different link frequencies (a) f = 20 kHz, (b) f = 40 kHz and (c) f = 80 kHz.

5.1.5 Effect of DC Source Voltage Variation on Compensation

From the previous study we observe that RDCLI is able to compensate the load harmonics. The compensated source current is almost sinusoidal except for some notches at the peak of the compensated current. This can be explained as follows, as the phase of the compensated source current coincides with that of the source voltage, the voltage difference between the inverter and the source is minimum during the period when these notches are present. Thus to force a current rapidly through interface inductor L_f a high di/dt is required. This can only be achieved by increasing V_{dc}. Fig. 5.4 shows compensated currents and the reference currents from the source at three different values of dc source voltages, namely, 385 V, 435 V and 470 V.

These simulations are carried out for a link switching frequency of 20 kHz. The notches present in Fig. 5.3 disappear with an increase in the dc source voltage. However there seems to be slight increase in chattering in the compensated current waveform in the other regions of the sinusoidal waveform. This is obvious as higher voltage increases change of current through the interface inductor, especially when the voltage difference across it is large.

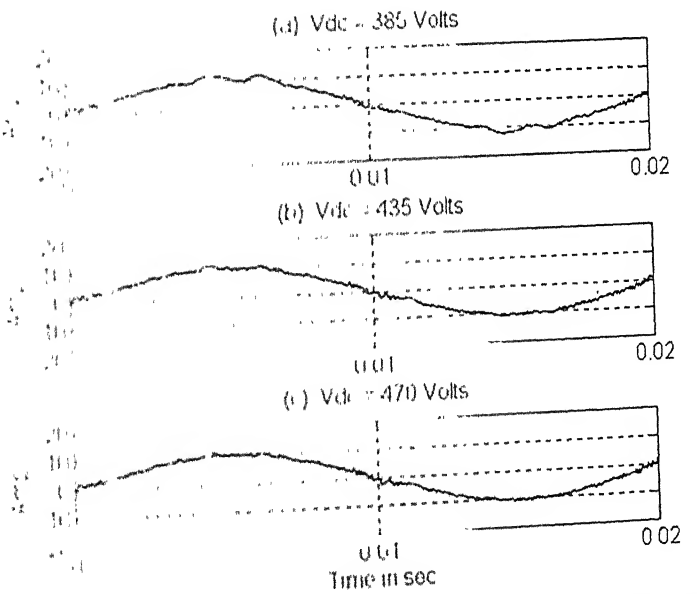


Fig. 5.4 Compensated currents from source at (a) Vdc=385 Volts, (b) Vdc = 435 Volts and (c) Vdc = 470 Volts

5.1.6 A Case Study

Having studied the effects of dc bus voltage variation and link frequency variation on the performance of compensator, a case study has been taken up when the compensator supports a typical non-linear load. In this simulation dc bus voltage chosen as 435 Volts and the link frequency chosen is 20 kHz. The load is assumed to draw current from the supply source that contains all the odd harmonics starting from 3rd till 23rd. It is to be seen how the compensator performs with the parameters chosen earlier. The simulated load current is shown in Fig. 5.5. The performance of the AHCC depends on the tracking ability of the inverter. Fig. 5.6 shows the inverter reference current and its tracking. It is seen that RDCLI is capable of tracking this fast changing waveform. Fig. 5.7 shows the compensated current from the source and the reference source current. From this figure it can be inferred that RDCLI based AHCC compensates all the harmonics. The ripples in the compensated current are minimum. The performance of the compensator can be judged by its ability to reduce the harmonic components of the supply current to a minimum. Fig. 5.8 shows the spectral response of the uncompensated system and that of the compensated system.

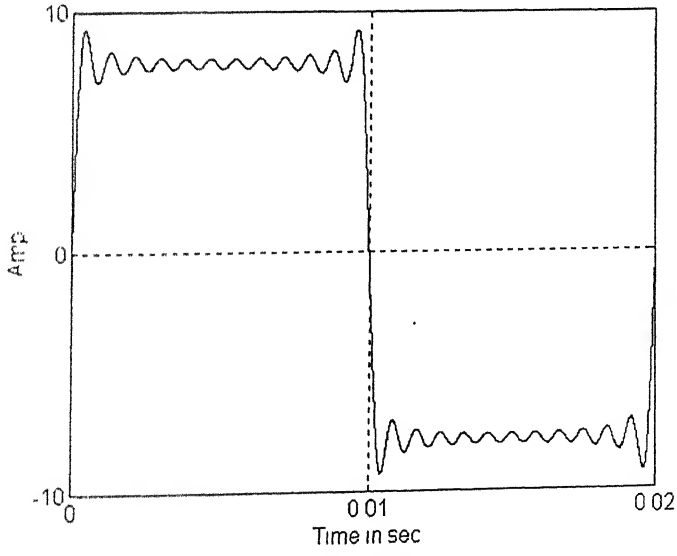


Fig. 5.5 Simulated load current

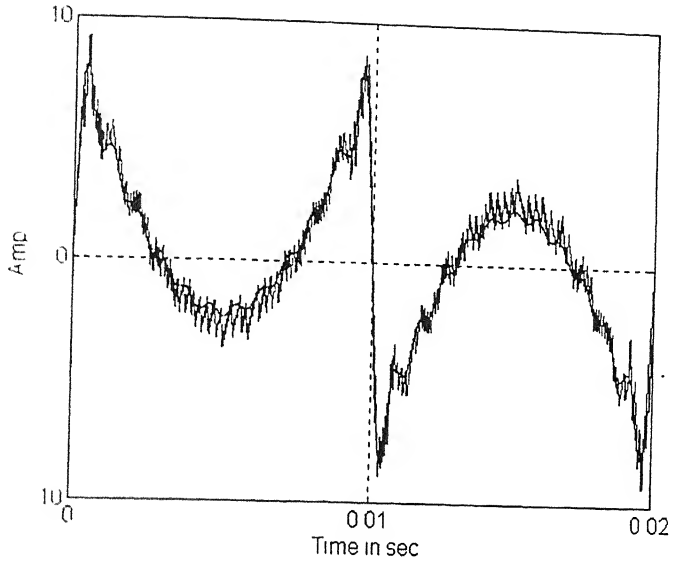


Fig. 5.6 Reference current for inverter and its tracking

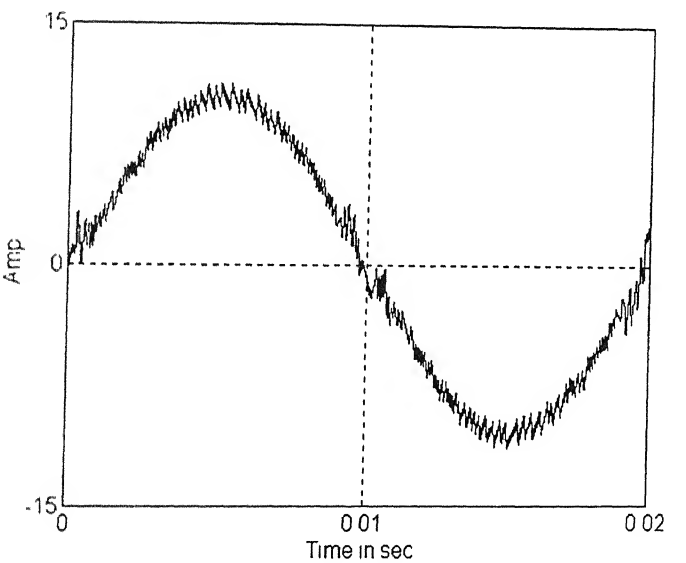


Fig. 5.7 Compensated source current

Let us consider the improvement in total harmonic distortion before and after connecting the AHCC. The THD in the load current is 46.14 %, which implies that this is the distortion in the source current in the absence of the AHCC. The THD reduces to 2.1 % after connecting the AHCC. The requirements specified by the utilities [46] usually are that the THD should be below 5 % and any single frequency component should be below 3 % of the fundamental. Both the above conditions are satisfied by this

AHCC. The THD in the compensated source current is usually treated as a figure of merit for any compensator, in this regard this compensator can be considered to be very good.

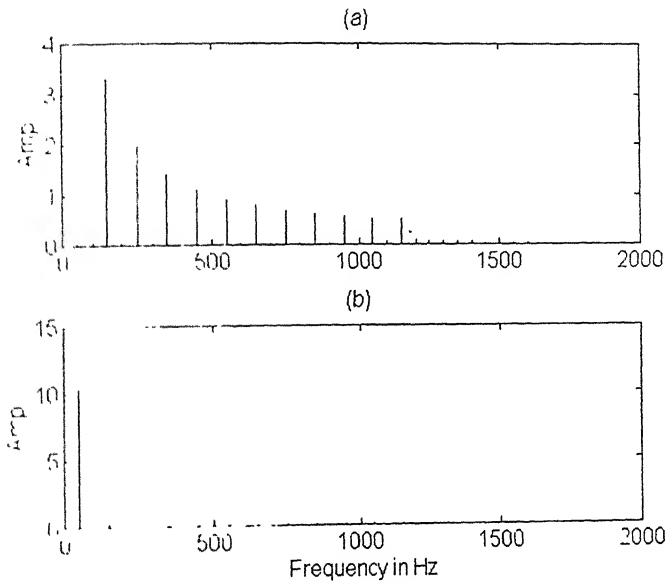


Fig. 5.8 Spectral response of (a) Load current, (b) Compensated source current

5. 2. QUASI-RESONANT DC LINK INVERTER BASED AHCC

From the previous section we observe that a judicious choice of dc link voltage and frequency is required for achieving compensation. However, it is found that the dc link voltage must be reasonably high. With a quasi-resonant dc link inverter (QRDCLI) it is possible to modulate the average dc link voltage to certain extent. Moreover, the switching frequency would be low compared to that of an RDCLI.

Here an active filter based on a high frequency quasi-resonant dc link inverter for current harmonic compensation is presented. Compensation principle is similar in the sense that we use this as a shunt compensator for injecting anti-phase harmonics into the line such that the load harmonics are cancelled. We propose a simple proportional controller for controlling the average dc link voltage and effective switching frequency so that inverter current closely follows its reference current. This compensator is particularly suitable for higher order harmonic compensation where a PWM inverter based compensator fails. The proposed solution is validated through extensive simulation results.

5.2.1 QRDCLI Topology

The QRDCLI topology was proposed by Lai and Bose [47]. The circuit is reviewed here. This topology is the same as that of a parallel RDCLI circuit except that a diode and a switch are added in series with the resonant capacitor as shown in Fig. 5.9. As with an RDCLI the link voltage goes through periodic zero crossings during which switching transitions are carried out, and I_0 represents current drawn by the inverter (switching network) which is actually the load current of the inverter. Also shown in this figure the shorting switch S_0 and the switch-diode pair (S_q, D_q), the function of which is explained below.

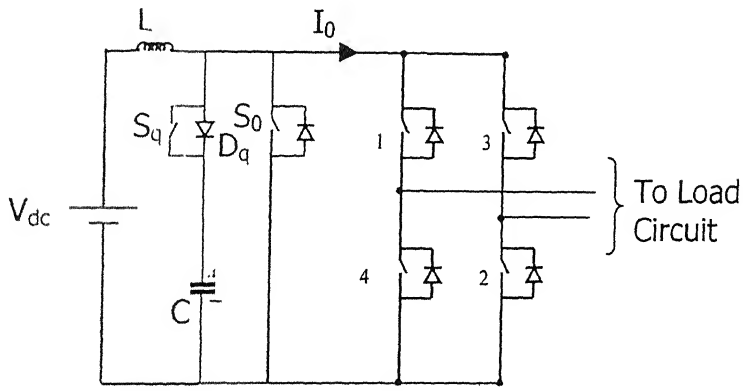


Fig. 5.9 Schematic diagram of single-phase QRDCLI

5.2.2 Equivalent Circuit of QRDCLI

The equivalent circuit of a QRDCLI is shown in Fig. 5.10 and its voltage and current waveform for one resonant cycle are shown in Fig. 5.11. Referring to Fig. 5.11, the link voltage v_{link} increases from zero to near $2V_{dc}$ in the first half of the resonant cycle. The link current i_R goes to zero about the same time when the link voltage peaks. The diode D_q blocks the current from going negative if the switch S_q is open. During this time the capacitor C is bypassed and the link voltage equals to V_{dc}. When the switch S_q is closed after a time delay of t_d, the link voltage is allowed to fall to zero. By controlling t_d we can control the average value of the link voltage to a desired level. This is followed by current initialization mode so that the link voltage goes to zero in the next

resonant cycle. The interval in which the dc link voltage is constant is termed as flat region.

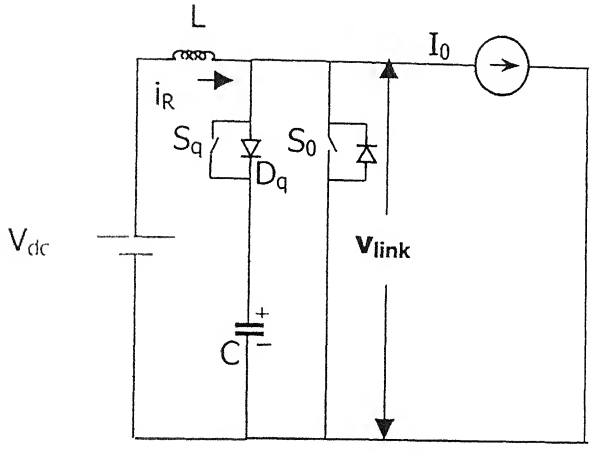


Fig. 5.10 Equivalent circuit of QRDCLI

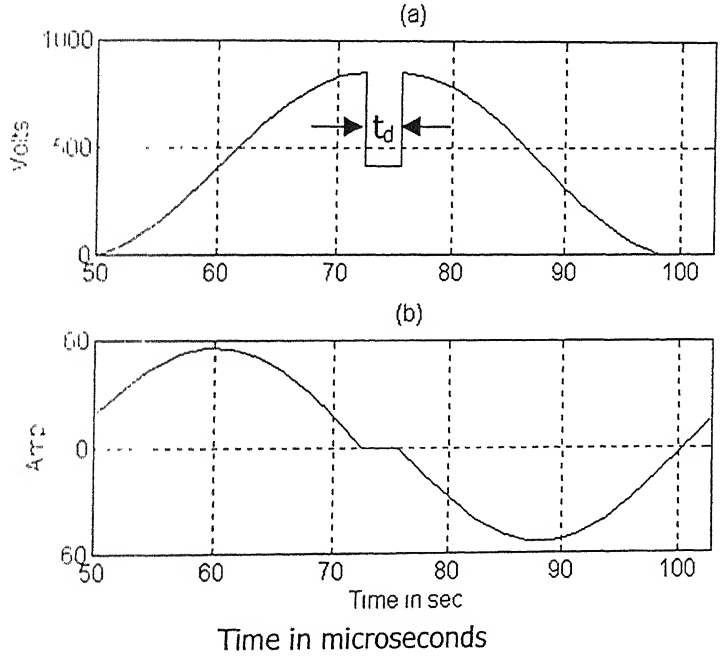


Fig. 5.11 QRDCLI (a) Link voltage, (b) Link current waveform

5.2.3 Principle of AHCC

The same principle is followed for the purpose of compensation as in the case of RDCLI discussed in previous section.

5.2.4 Operation and Control of AHCC

As mentioned before, the basic philosophy of AHCC is to generate a non-sinusoidal current following a command. The control of QRDCLI based AHCC comprises of three parts. These are:

- Choosing a proper time interval for the flat region as depicted in Fig. 5.11.
- Choosing a proper value of initial current to avoid zero crossing failure in QRDCLI.
- Current tracking.

5.2.5 Controlling the Flat Region

As mentioned earlier that an RDCLI based compensator performs well at a higher dc link voltage. Further the notches around the peak of the input source current reduce substantially using a higher value of dc link voltage. However, there is more chattering in the current waveform in other regions. It is thus desirable to increase the average link voltage by a small amount rather than boosting V_{dc}. It is thus important to control the time delay t_d such that the average voltage can be modulated according to requirement. For this we use a simple proportional controller [48]. As mentioned earlier, this time delay is controlled by opening and closing the switch S_q. Normally this switch is kept open. Therefore the resonant circuit current flows through the path formed by V_{dc}, L, diode and C. When the current in this path becomes negative, the diode D_q blocks. During this state the resonant current is zero and the link voltage equals to dc source voltage. After allowing a suitable time delay t_d switch S_q is closed. The resonance restarts, now through the path V_{dc}, L, S_q and C. This switch is maintained in the on state till the current becomes positive, then the diode D_q across the switch will take

over. The switch S_q is then turned off. To control this time interval, let us define an error function as

$$e_t = i_f^* - i_f \tag{5.1}$$

where i_f^* is the reference and i_f is the actual compensator current. We then use the controller to get the time delay t_d. This is given by

$$t_d = K_p' e_t \tag{5.2}$$

where K_p' is the proportional compensator gain and e_t is the error function as mentioned earlier. The gain K_p' is chosen such that the time delay t_d is kept within a few microseconds. In this control scheme it is possible for t_d to become positive or negative depending upon the sign of e_t. The error becoming negative implies that the link voltage is high. However, there is no mechanism to reduce the voltage. Thus t_d is forced to zero instead. This is accomplished by switching S_q on immediately such that flat region does not appear in the voltage waveform.

5.2.6 Current Initialization Technique

The introduction of the time delay t_d does not alter the current initialization scheme discussed in Section 3.2. Refer to Fig. 5.11 from which it is evident that during the time t_d the diode D_q blocks the current i_R to maintain it at zero. Therefore the voltage across the link is also maintained at the level V_{dc} for the time for which i_R is zero. When the switch S_q is turned on the current is allowed to go negative and as a result the voltage starts converging towards zero. Thus even though the time for which link voltage is non-zero is $\Delta T + t_d$, the time duration for resonance remains unaltered. Therefore equations used in Section 3.2 for current initialization are still valid.

5.2.7 Current Tracking

The zero-hysteresis bang-bang control described in Chapter 3 is used for current tracking in this case also.

5.2.8 Results with QRDCLI based AHCC

The QRDCLI based active harmonic current compensator is simulated using the MATLAB software package. All the simulations are carried out for a single-phase system. The system parameters chosen are:

- Interface Circuit: $L_F = 15\,mH$, $R_F = 0.2256\,\Omega$.
- AC Supply: $v_s = 440\sqrt{\frac{2}{3}}\sin(100\pi t)$.
- Resonant Circuit: $R = 0.0531\,\Omega$, $L = 63.32\,\mu H$, $C = 1\mu F$, $V_{dc} = 385\,V$.
- Proportional Controller: $K_p' = 20\ \mu s$.

The link frequency chosen is 20 kHz. The load is assumed to be non-linear that contains 3rd, 5th, 7th, 9th, 13th and 23rd harmonics in addition to the fundamental. It is to be noted that this is not a specific power-electronics load and only chosen as a test signal. Different types of components are included to see how well these harmonics can be compensated. The magnitudes of the harmonic components with respect to the fundamental are inversely proportional to the harmonic number. The load current is shown in Fig. 5.12.

Fig. 5.13 shows the reference current and tracking current of the compensator. It is clear that the compensator is capable of tracking a highly nonlinear and fast varying current. Fig. 5.14 shows reference source current and the compensated source current. It is observed that a nearly sinusoidal current flows from the source after compensation. There are some small notches around the peak value of the compensated source current.

It is observed that QRDCLI based compensator compensates load harmonics. The amplitude of different harmonic components in the load current and compensated source current are shown in Fig. 5.15. The total harmonic distortion (THD) of the same current in the absence of the compensator is 43.78 % while it is reduced significantly to 4.71 % after compensation. An RDCLI based AHCC for the same load, operating at same frequency and dc voltage has a THD of 4.8 %.

It is thus found that the performance of this AHCC is marginally better than that of an RDCLI based AHCC. However, we need an additional switch and controls. Moreover, the switching on and off of this switch would result in further losses in the

system. The marginal reduction in THD does not justify the additional complexity. Therefore we shall concentrate only on RDCLI based AHCC for single-phase loads.

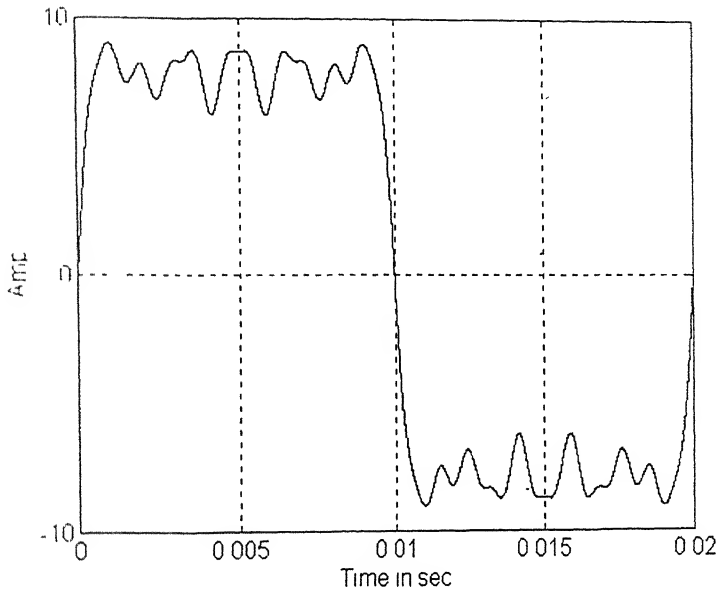


Fig. 5.12 Simulated load current

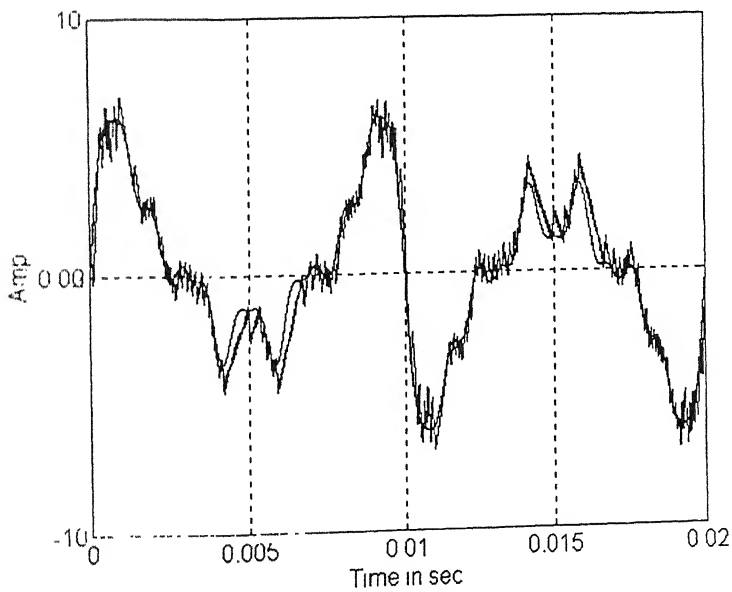


Fig. 5.13 Compensator reference and its tracking

driven by a fixed dc source. We have concluded that an RDCLI is superior to a QRDCLI from the circuit complexity and switching loss points of view. We shall therefore use RDCLI for further investigation.

In this section, we use an RDCLI based AHCC that is driven by a dc storage capacitor. For simulation studies the capacitor charge control algorithm is same as that given in Section 2.2 except that it is used for a single-phase system. The system parameters chosen are:

- Interface Circuit: $L_f = 15\text{mH}$, $R_f = 0.2256\Omega$.
- AC Supply: $v_s = 440\sqrt{\frac{2}{3}}\sin(100\pi t)$.
- Resonant Circuit: $R = 0.0531\ \Omega$, $L = 63.32\ \mu\text{H}$, $C = 1\mu\text{F}$.
- PD Controller: $K_p = 200, K_D = 40, N = 20$.

The value of the energy storing capacitor is chosen as 2000 μF. It is assumed that the capacitor is initially pre-charged to 435 Volts.

The simulated load current is non-linear; it contains all odd harmonics (from 3rd till 23rd). The magnitude of the fundamental component is 10 A and the harmonic components are of magnitudes which are inversely proportional to their harmonic number. The simulated load current is the same as shown in Fig. 5.5.

Zero-hysteresis bang-bang control is used for current control of the inverter. The compensator reference current and its tracking are shown in Fig. 5.16. It is observed that inverter is able to produce the desired current so that the tracking error is minimal. The compensated source current from the source is shown in Fig. 5.17. It is seen that the source current is sinusoidal except for high frequency ripples. This is due to high frequency switching. It is also observed that the delay due to the controller is about one cycle. The capacitor voltage is potted in Fig. 5.18. The capacitor voltage settles to its steady state value after 1 cycle.

The performance of the AHCC in conjunction with the PD controller is quite good. The superior features of this compensator are:

- Fast transient response (one cycle delay)
- High efficiency (zero or minimum switching loss)
- Simple control

- Adequate current regulator bandwidth (capable of tracking fast changing currents)

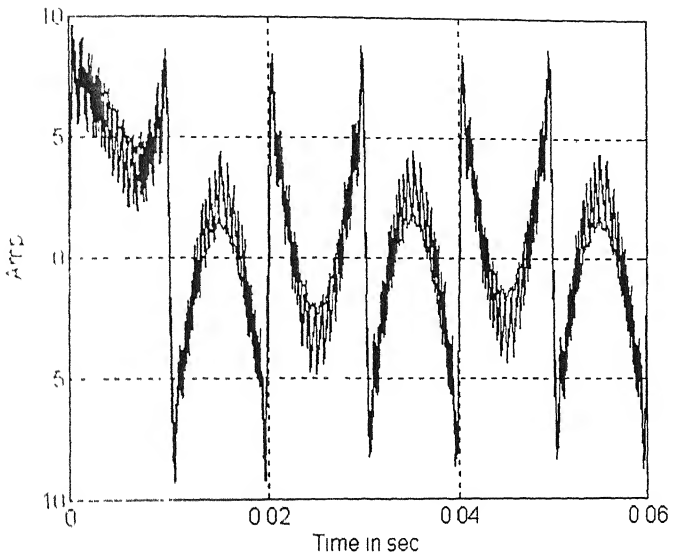


Fig. 5.16 Compensator reference and its tracking

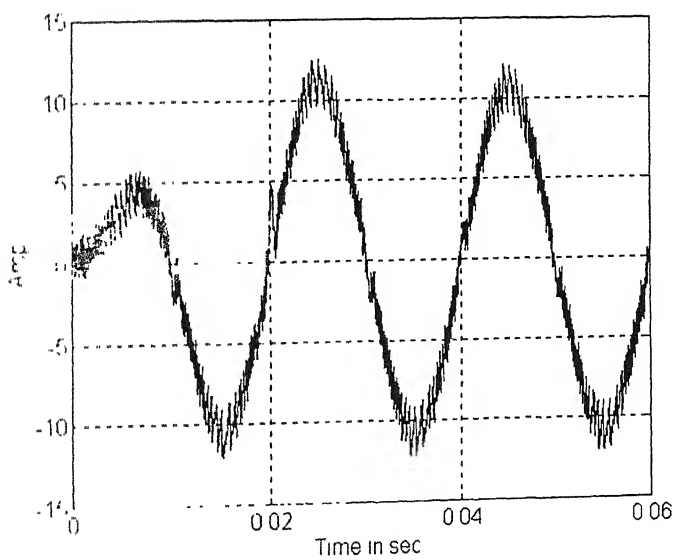


Fig. 5.17 Source current after compensation

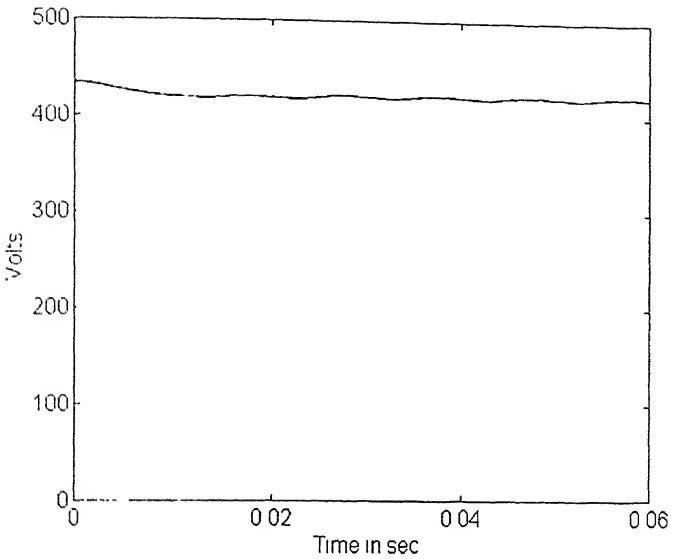


Fig. 5.18 DC Voltage across capacitor

5.4 THREE-PHASE AHCC USING THREE SINGLE-PHASE INVERTERS

It is mentioned that a single-phase soft-switched inverter is superior to its three-phase counterpart for AHCC application. In this section we propose a topology by which three single-phase inverters are used for compensating harmonics in three-phase loads.

The compensating system is shown in Fig. 5.19. On the dc side of the AHCC we have a single dc capacitor that also supports the resonant link. The link voltage feeds the three inverters. The ac sides of the inverters are connected to the system bus through isolation transformers as shown in Fig. 5.19. Isolation transformers rather than interface inductors are used in this case to avoid shorting of the dc bus.

The quantity I_0 of the resonant link is obviously dependent on the three inverter currents and their respective switching conditions. Therefore, current initialization that is done in every resonant cycle, will depend on I_0, which is now computed from the three compensator currents and switch condition of three inverters. In addition, the dc capacitor voltage is also used in current initialization. The current initialization is done as described in Chapter 3 (Section 2).

The load is such that phase-a and phase-b carry 10 A (peak) current and are phase displaced by 120°. In addition, these currents also contain odd harmonics up to 25th order minus the triplens. The third phase of the load is open. The objective of the compensator is to achieve both harmonic compensation and load balancing.

We use the PD controller for extraction of compensator reference. Because of the unbalance and harmonics the capacitor is likely to experience large ripple. To minimize the ripple we use a lower value of cut-off frequency for the LPF. We first present results with a cut-off frequency $f_n = 20$ Hz where $\omega_n = 2\pi f_n$ rad/sec. The LPF transfer function is

$$G_{LPF}(s) = \frac{\omega_n}{s + \omega_n} \tag{5.3}$$

The reference source currents extracted by the PD controller for the three phases are shown in Fig. 5.20. The currents become almost balanced after 7 to 8 cycles. However little unbalance still exist due to ripple in the PD controller output. Now the cut-off frequency (f_n) is further reduced to 10 Hz. The reference source currents for this case are plotted in Fig. 5.21. The source currents are now completely balanced. There is a delay of about 12 to 13 cycles as the controller convergence is slowed down by the presence of LPF with low cut-off frequency. The controller output is shown in Fig. 5.22. The dc capacitor voltage is plotted in Fig. 5.23. It is seen that some ripple in the control output still persists. This is unavoidable with this LPF configuration. To eliminate the ripple altogether better filter design may be investigated. The compensated currents from source for two cycles are shown in Fig. 5.24. These currents are sinusoidal, balanced except for some high frequency ripple. This establishes the effectiveness of the AHCC. We therefore can safely conclude that a single-phase soft-switched AHCC is much-preferred topology than its three-phase counterpart as we can use three such inverters to compensate three phase loads effectively.

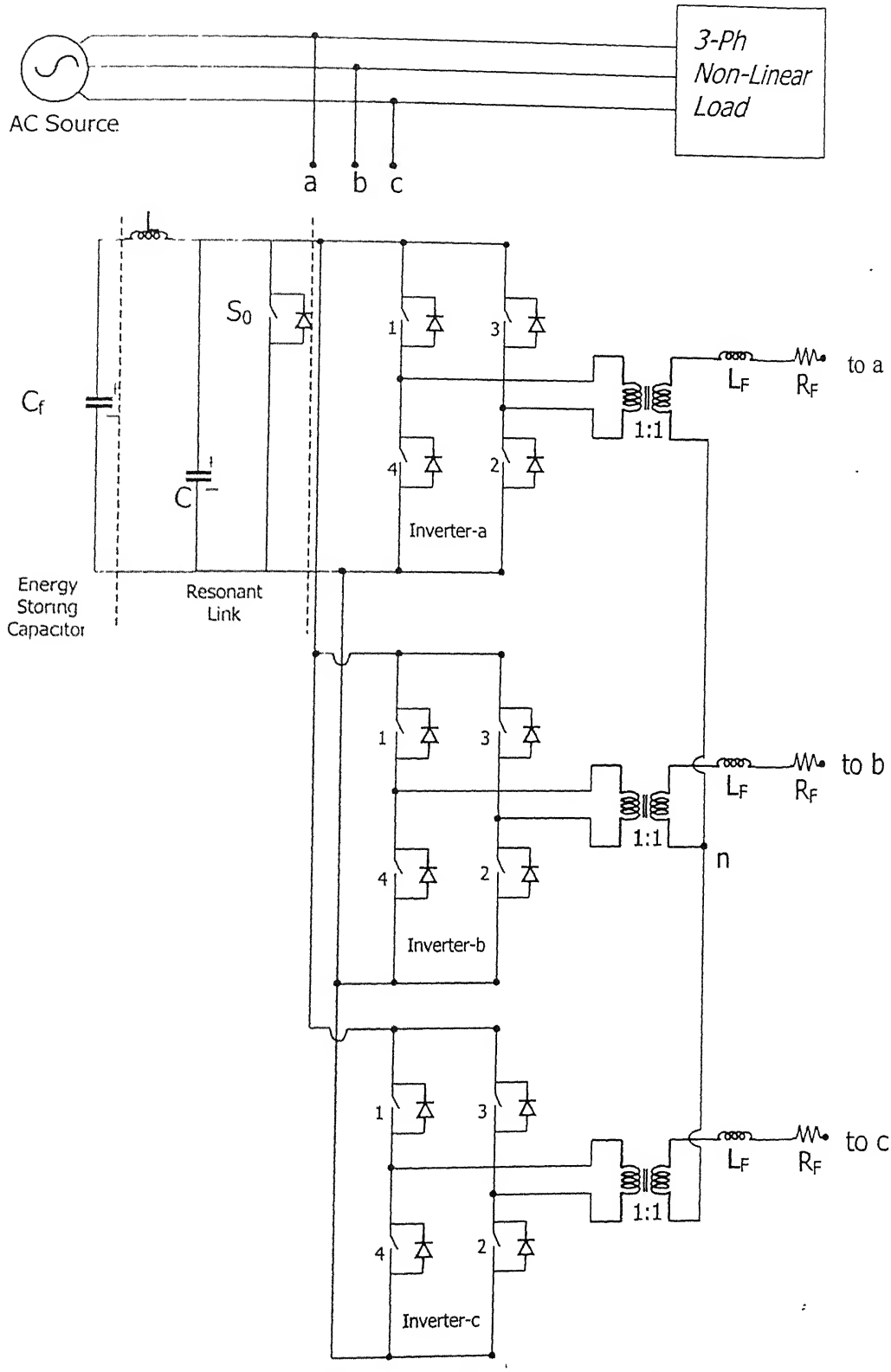


Fig. 5.19 Three-phase AHCC using three single-phase inverters

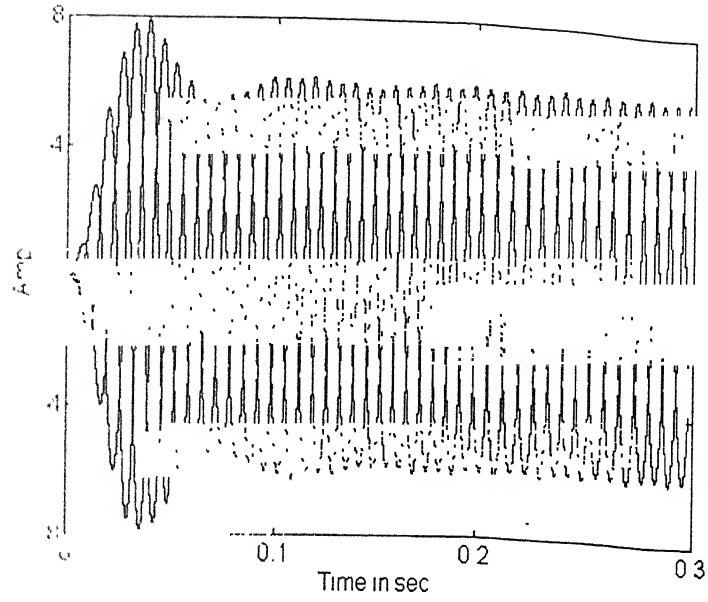


Fig. 5. 20 Three-Phase reference currents under unbalanced load conditions and at f_n =20 Hz.

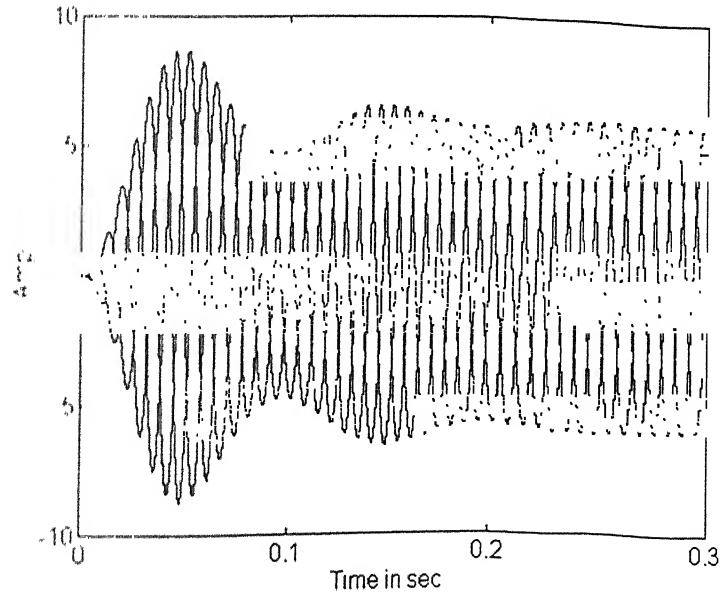


Fig. 5. 21 Three-Phase reference currents under unbalanced load conditions and at f_n=10 Hz.

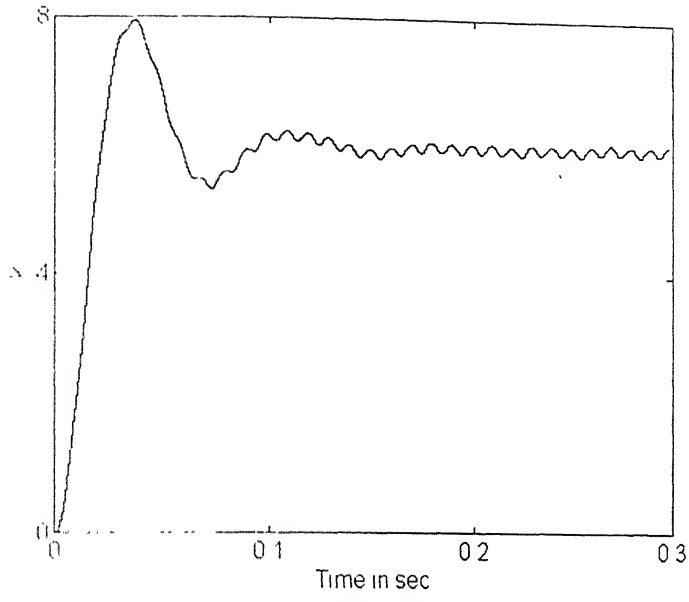


Fig. 5.22 PID Controller output under unbalanced load conditions and at f_n =10 Hz.

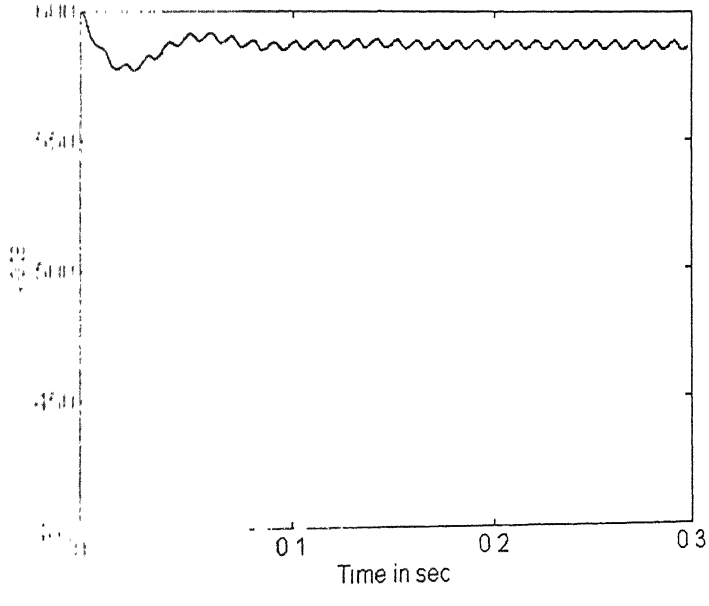


Fig. 5.23 DC Capacitor voltage under unbalanced load conditions and at f_n =10 Hz.

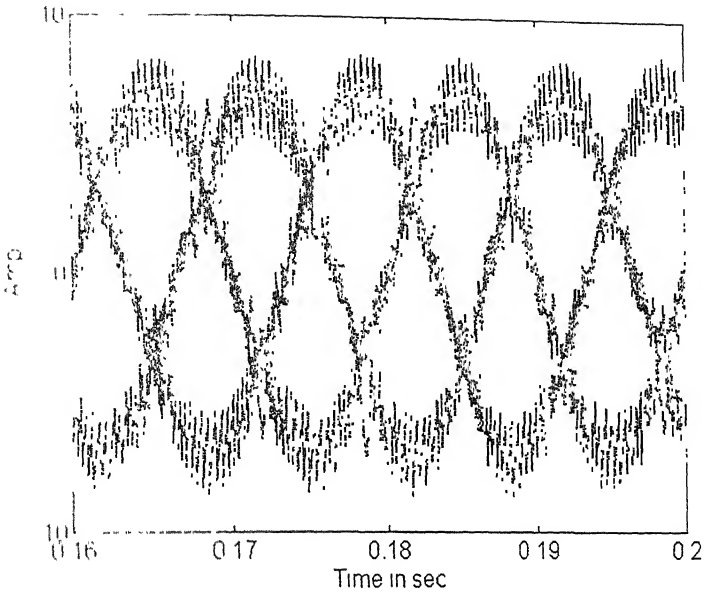


Fig. 5.24 Three-phase compensated source currents under unbalanced load conditions and at f_n =10 Hz.

5.5 CONCLUSIONS

The study of Resonant DC Link Inverter as an active harmonic current compensator reveals that it is possible to compensate the harmonic currents generated in the source by the non-linear loads. The simulations indicate that THD and different individual harmonics in the compensated current are well below the limit prescribed by the power utilities. A judicious choice of the level of link voltage and its switching frequency of the inverter makes the compensator perform better. The compensator in conjunction with the PI controller is shown to provide fast response to changing load conditions. The compensator can be designed for high power level depending upon the availability of fast switching high voltage and high current devices such as IGBTs.

The study of Quasi-Resonant DC Link Inverter as an active harmonic current compensator reveals that it is possible to compensate the harmonic currents generated in the source by the non-linear loads. The simulations indicate that THD and different individual harmonics in the compensated current are well below the limit prescribed by the power utilities. QRDCLI based compensator performance is comparable with

RDCLI based compensator. However the requirement of additional switch tends to make the system more complex.

It is possible to realize a three-phase AHCC using three single-phase inverters that are energized by a single capacitor. The performance of this AHCC is found to be quite good even under adverse load conditions.

CHAPTER 6

EXPERIMENTAL SETUP

The experimental used for experimental verification of AHCC principle is discussed in this chapter. The objective is to demonstrate the performance of single-phase AHCC based on both hard and soft-switched inverters. For RDCLI based AHCC a resonant link is fabricated which is controlled by the proposed current initialization scheme that includes PC interface. In this chapter the details of fabrication of various control cards, the power circuit, the drive circuit of the inverter and the PC interface are given.

The power circuit of the RDCLI based AHCC is shown in Fig. 6.1. The ac supply supplies the non-linear load. The RDCLI acts as the compensator. The capacitor (C_f) in the circuit is the energy storing capacitor. The diode-bridge and the inductor are used for pre-charging. Once charging is done, this part of the circuit is opened using a mechanical switch MS-1. The block diagram of the RDCLI based AHCC is shown in Fig. 6.2.The capacitor voltage is sampled through a Hall-Effect voltage transducer and this is given to the controller circuit. The compensator reference is obtained from this circuit. This signal is given to the current regulator circuit such that current regulator provides the required current. Current initialization is carried out as described in current initialization circuit for ZVS purpose.

The power circuit for the PWM inverter based AHCC is shown in Fig. 6.3. The essential difference from the previous circuit is that here we use PWM inverter as power circuit. The current regulation within the inverter is done through PWM controller card.

6.1 FABRICATION OF RESONANT LINK

The power circuit of the resonant link is shown in Fig. 6.4. To pre-charge the capacitor C_f a diode-bridge is used along with a filter inductor. Through the diode-bridge we can build up the voltage V_{dc} across C_f which will act as a supply for the resonant link. The resonant link consists of inductor L and capacitor C. In order to get high Q factors for the inductors at high resonant frequencies a litz-wire air core inductor is fabricated. The design and fabrication of these air core inductors [49] are given in appendix A. The resonant link capacitor is of polypropylene type while the filter capacitor C_f is electrolytic type. The link is designed to operate at a frequency of 23.4 kHz for which the various resonant component values are L = 52 μH, C = 0.89 μF, C_f = 3000 μF, Q = 60, V_{dc} 65 V. A careful physical layout of the resonant components has been made. It is to be noted that a variable external resistance R_{ext} is added in series with the shorting switch S_0. This is done for protection and is used during the starting stage. Once the link starts up and operational this is reduced to zero.

6.2 CURRENT INITIALIZATION CIRCUIT

With these values of inductor and capacitor the undamped oscillation time is 42.75 μs. Therefore, the resonant cycle time ΔT is chosen to be 37.5 μs taking into account the finite Q-factor of the coil.

The block diagram of the proposed current initialization scheme is shown in Fig. 3.5. The corresponding control circuit is shown in Fig. 6.5.

A Pentium personal computer (PC) along with its associated high-speed analog-to-digital converter (ADC) and digital-to-analog converter (DAC) is used for the computation of the initial current from equation (3.4). In this equation θ_{11}, θ_{21} and ϕ_{21} are constants that are dependent on the circuit parameters and the time ΔT. These are pre-computed and stored. The load current (I_0) and the dc voltage V_{dc} are measured through Hall-effect sensors (HE-1 and HV-1 respectively in Fig. 6.1) at the start of every resonant cycle (e.g. t_2 in Fig. 3.3) and are converted through ADC. These measured values along with the constants mentioned above are used for the computation

of the initial current. This process is repeated for every resonant cycle. It is to be noted that the computation here is fairly simple and can also be achieved through a hardware configuration. However, the use of PC makes the control circuit much more flexible than a hardwired circuit. Furthermore, due to the presence of the PC, the delays and tolerances of the actual circuit can also be taken into account. An accurate zero-voltage switching can be obtained in the experiment.

As mentioned in Chapter 3 (Section 3.2) there are two methods of obtaining time Δt for which the capacitor should be shorted, of which we use method-2. As soon as the required initial current is computed in the PC, it is converted into an analog signal through a DAC. The computation time required is much smaller than the resonant cycle time ΔT. This signal is then available to the comparator for comparison with the actual link current. The link current is monitored continuously through a Hall-effect current sensor (HE-1 shown in Fig. 6.4). Let us discuss the operation of the circuit in Fig. 6.5. When the link current becomes equal to the required initial current, the comparator output (Y) becomes zero. The signal Y is conditioned by protection circuit (Fig. 6.6) and then the output Z= Y P_t is used for clearing the J-K flip-flop (74LS76 in Fig. 6.5). Under normal condition Z= Y, as protection signal P_t = 1. Once this flip-flop is cleared, its output (Q) becomes zero and $\overline{Q}$ becomes one. This is then used for switching off S_0 through a buffer. Simultaneously, the inverted output ($\overline{Q}$) of the J-K flip-flop is used for triggering the monostable (7555 in Fig. 6.5) through an inverting buffer. The monostable timing is designed for a pulsewidth of ΔT=37.5 μs. After this time elapses, the negative going edge of the monostable output is used to clock the J-K flip-flop. This forces the output of the flip-flop to one and consequently the shorting switch S_0 is turned on.

Through the above scheme, the zero-voltage switching is obtained. It is to be noted that during the time when S_0 is on, the switching transitions of the switches $S_1 - S_4$ take place. To ensure that the switches $S_1 - S_4$ are turned on or off only during this prescribed interval, the gating of $S_1 - S_4$ are conditioned by the output Q of the J-K flip-flop. Further note that the configuration of the switches $S_1 - S_4$ at a particular resonant cycle is dependent on the load connected to the output of the inverter. It is to

be noted that the J-K flip-flop is cleared under two conditions. One is the usual clearing as explained already in every resonant cycle. The other is under fault condition. If there is a fault, the resonant circuit must be stopped. In that case the protection circuit gives $P_t = 0$ and signal Z is forced to zero. The switch S_0 is therefore opened permanently so that the link voltage and link current will gradually decay to zero due to the internal resistance of the resonant coil. The output of the monostable is also used for the starting ADC. When this is triggered through $\overline{Q}$, its output goes high. This is also the onset of the resonant cycle. This positive going edge (through buffer CD 4049) is used as a signal to the PC interface card such that the ADC starts sampling I_0 and V_{dc}.

6.3 CURRENT REGULATOR CIRCUIT

The current regulator control circuit is shown in Fig. 6.6. The switching of the devices is synchronized to the zero crossings of the link voltage so as to obtain ZVS. The resonant dc link inverter and controller is configured to regulate its current so as to match the current reference. As mentioned earlier the monostable of Fig. 6.5 is triggered at the onset of a resonant cycle. This then goes zero after 37.5 μs elapses. The negative going edge of the monostable output is used for clocking the J-K flip-flop. This forces the output of the flip-flop to one and consequently the shorting switch S_0 is turned on.

The same signal is used to clock the D-flip-flop (74F74) in Fig. 6.6 so that the synchronization is obtained. The comparator compares the actual inverter current (HE-III) with the reference of the inverter (obtained from the PD controller card). Based on the output of the comparator (LM-311), a switching decision has to be taken. This output is fed to the D input of the D latch. However, the output of the D flip-flop remains unaltered till the next sampling point is reached. The sampling point is the point when resonant link voltage goes zero. At this sampling point if the output current is lower, then a positive pulse is given to increase the output current and vice-versa. However, this pulse is not directly given as seen in Fig. 6.6. It is ensured that the outgoing switches are turned off first and then the incoming switches are turned on. This is achieved via monostable 74123 and AND gate 7408. Therefore a change from 0 to 1 in the 74F74 output is delayed by 1 μs where as a change from 1 to 0 in the 74F74 output is passed immediately.

For the protection of both resonant link and the current regulator a protection scheme is devised in this circuit. The load current is not allowed to be more than 4 A in either direction. This is done via two comparators. One comparator is set at 4 A and the other comparator is set at - 4 A. The actual current in the load circuit is compared with these references. Once the current is beyond limits of ± 4 A, one of the comparator output goes zero. This is then used for clocking a negative edge triggered J-K flip-flop. Therefore under normal conditions the $\overline{Q}$ output (P_t) of this J-K will be 1, this will go zero the moment current limit exceeds. This signal is used for blocking the gate signals. Manual resetting of the J-K flip-flop is required to clear the fault.

The signals derived for switches $S_1 - S_4$ are transmitted for gate drive circuit after being ANDed with current limit control signals. There is also a manual start/stop switch through which the circuit can be stopped at any time. The gating signals are also ANDed with the start/stop signals. Therefore under normal conditions the signals for switches $S_1 - S_4$ are passed immediately.

But under fault conditions these signals are blocked. This is achieved through AND gates 7408. The comparator output obtained from resonant link control circuit is also ANDed with this current limit control. In the event of a fault the J-K in current initialization circuit is cleared so that the switch S_0 is opened.

6.4 PD CONTROLLER CARD

The PD control circuit is shown in Fig. 6.7. It is to be noted that charge and voltage are directly proportional. Thus voltage is a good indicative of charge and vice versa. We use the voltage feedback for the PD controller. The dc capacitor voltage obtained through voltage transducer (HV-1) is put through a low pass filter. This quantity is compared to the capacitor voltage reference. This difference drives the PD controller. The output of the PD controller k is used to derive the reference for the source current. The reference waveform for the source is obtained through multiplication of k with sinωt (template of source voltage). The source voltage is first stepped down using a 230:6 transformer and is than scaled down to obtain sinωt signal using scale changer. Therefore we get a signal sinωt. This signal is multiplied using two AD-538 (ACU) with k. So that the source

current reference is generated. This line current reference is then subtracted from the load current (obtained from HE- IV). The resultant is the compensator reference.

6.5 PWM CONTROLLER AND BLANKING CIRCUIT

The circuit is shown in Fig. 6.8. The purpose of this circuit is to modulate current in PWM VSI. Therefore the task is to compute current error and generate switching signals for the inverter so as to regulate the error within the hysteresis band. The blanking circuit uses this signal to generate switching signals for all four switches. It is to be ensured that the outgoing switches are turned off first. The incoming switches are then turned on. Therefore a change from 0 to 1 in the 7400 output is delayed by 1 μs where as a change from 1 to 0 in the 74F74 output is passed immediately. This is achieved via monostable 74123 and AND gate 7408. It is to be noted that this 1 μs delay is sufficient to ensure that IGBTs are turned off. This is a mandatory requirement in PWM-VSI. Otherwise two switches in the same leg will be turned on resulting shorting of the dc bus. This is commonly known as shoot-through fault and this is avoided using this lockout scheme. The reference current that is to be tracked is obtained from controller circuit. Hysteresis band is generated by adding and subtracting the band. This is done through OP-AMP based adder and subtractor circuit. A hall-effect current sensor (HE-5) is used for the measurement of actual load current. This signal is then compared with the two references already generated. Based on the error signal a particular switch pair is fired and the other pair is turned off. It may be noted that when there is no need for changing the status of the switches the RS Latch holds the old status.

6.6 IGBT GATE DRIVE CIRCUIT

The circuit is shown in Fig. 6.9. A gate-drive circuit is designed in the similar lines as in [50]. The overcurrent - protection feature is added here. The protection scheme is based on the fact that the drain-source voltage of IGBT increases with drain current for a given gate-source voltage. The potentiometer P2 shown in the figure is set such that the voltage at variable point is one diode drop more than the drain source voltage corresponding to the peak value of the normal drain current. Activation of protection circuit is delayed by a RC circuit. As long as the drain current is within the normal limit,

the drive signal is transmitted to the gate. When the current exceeds its limits, the protection logic inhibits the drive signal from reaching the gate, and a fault indication is given. The fault indication persists as long as the turn-on process is present. An indication is also given in case of a turn-on failure.

6.7 PC INTERFACE CIRCUIT

For proposed current initialization scheme a PC is used as discussed earlier. Essentially two signals (the dc capacitor voltage and the load current seen by resonant link) are taken which are digitized using ADCs and then these data are used for computation. Once the computation is over, the required initial current value (through DAC) is sent to the current initialization circuit as shown in Fig. 6.5. Details of the interface card [51] are presented in appendix B.

6.8 CONCLUSIONS

In this chapter the details of different circuits that are fabricated is discussed. The photographs of the laboratory set up are shown in Fig. 6.10 through 6.14.

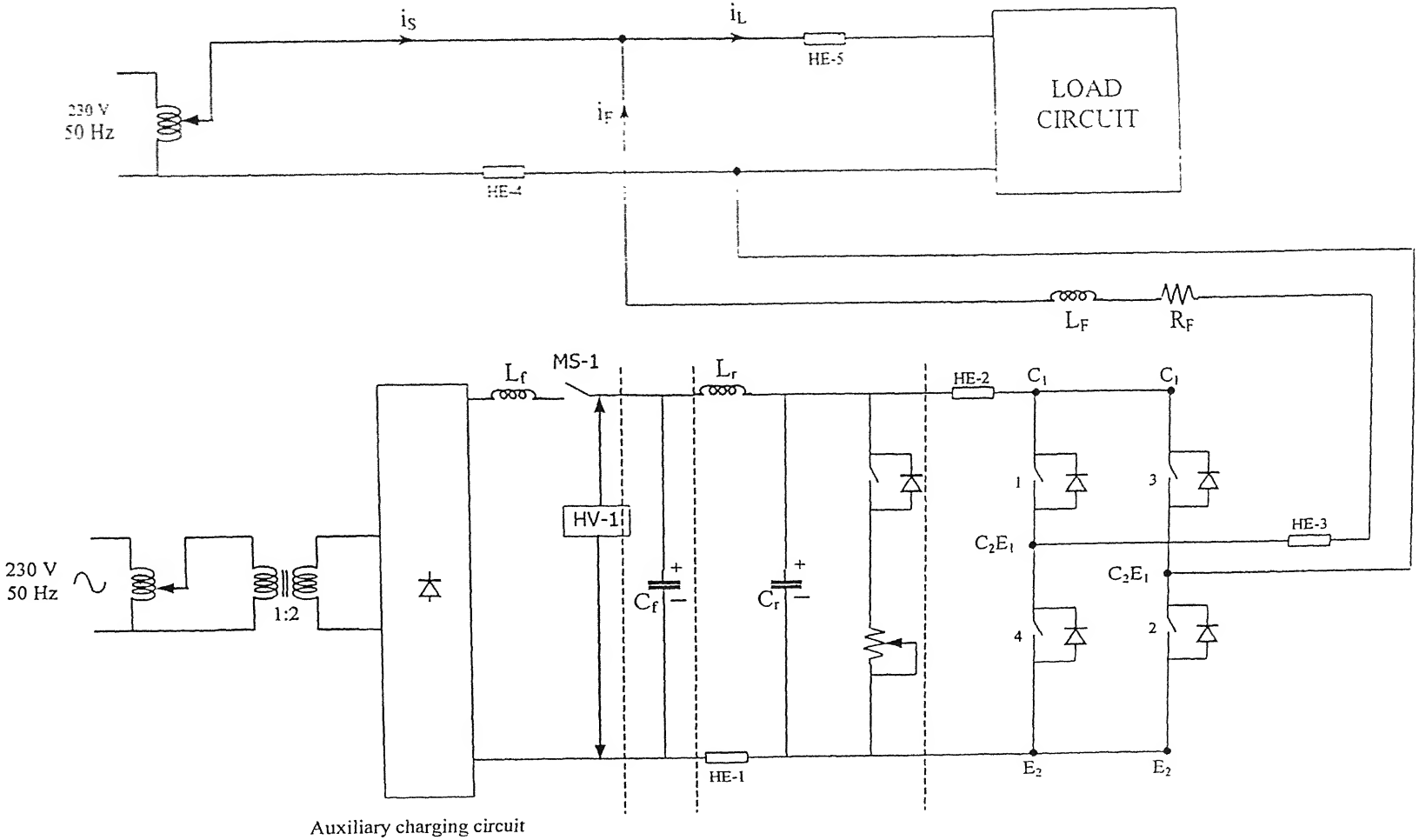


Fig. 6.1 Power circuit of RDCLI based AHCC

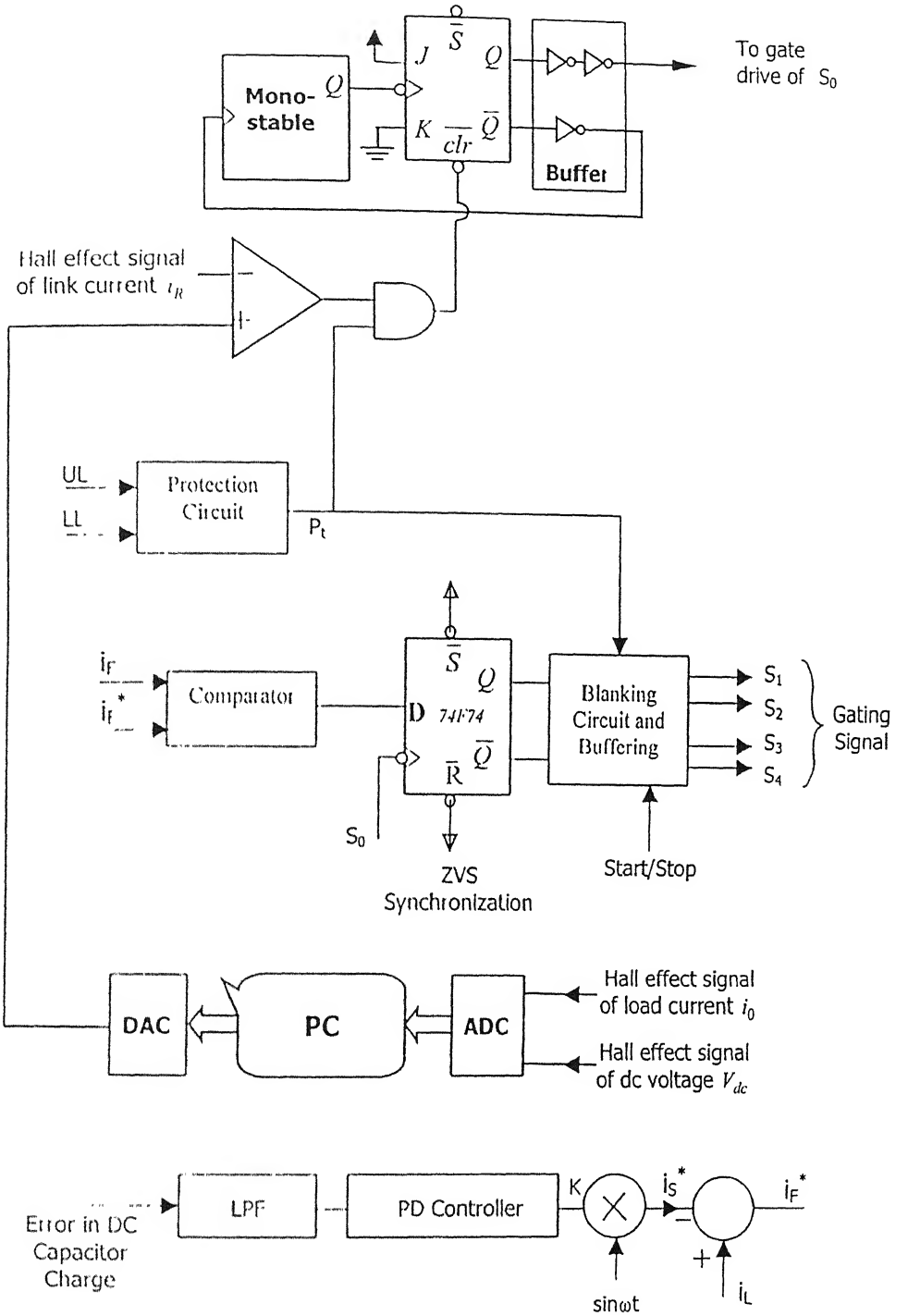


Fig.6.2 Block diagram of RDCLI based AHCC

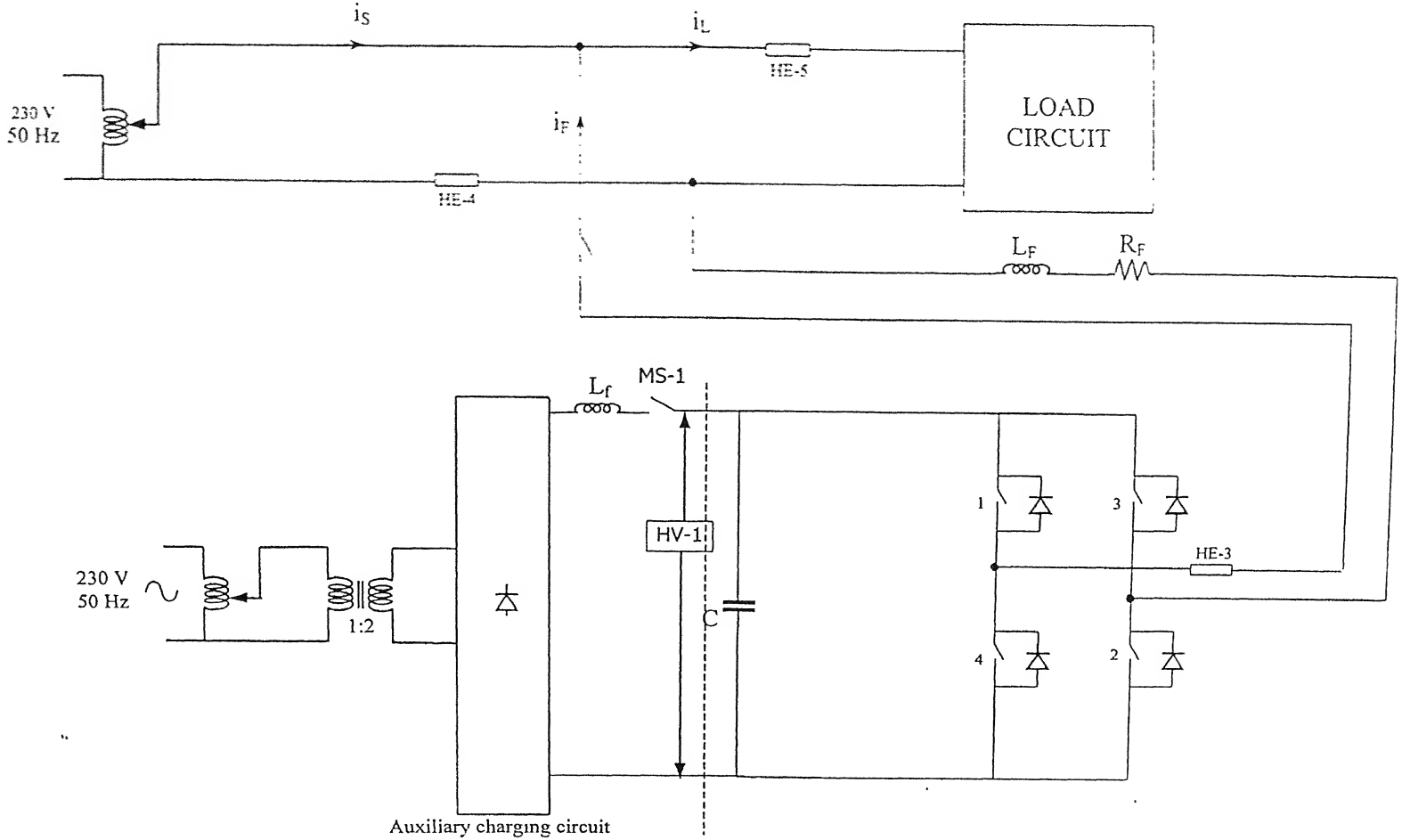


Fig. 6.3 Power circuit of PWM inverter based AHCC

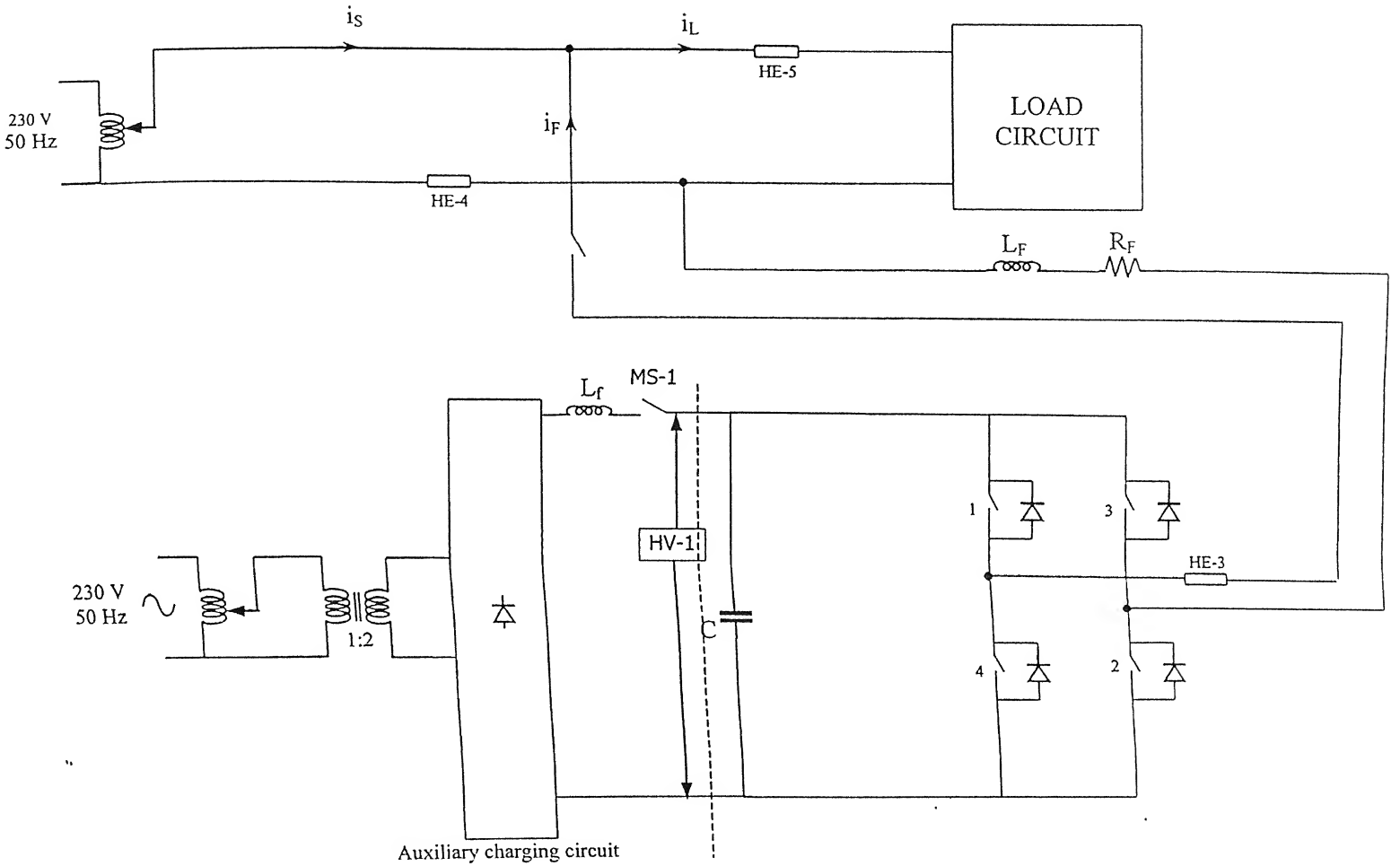


Fig. 6.3 Power circuit of PWM inverter based AHCC

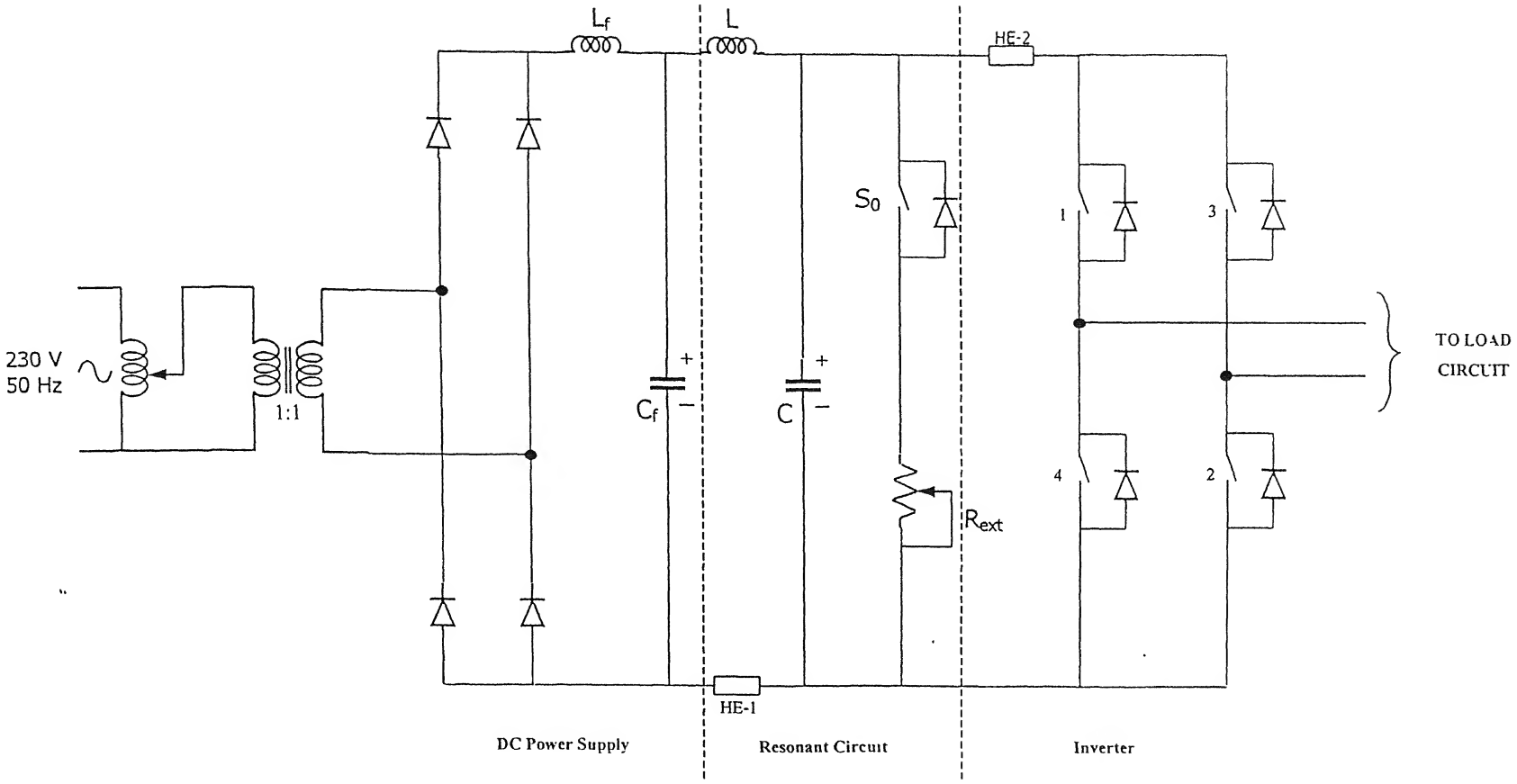


Fig. 6.4 Power circuit of resonant dc link inverter

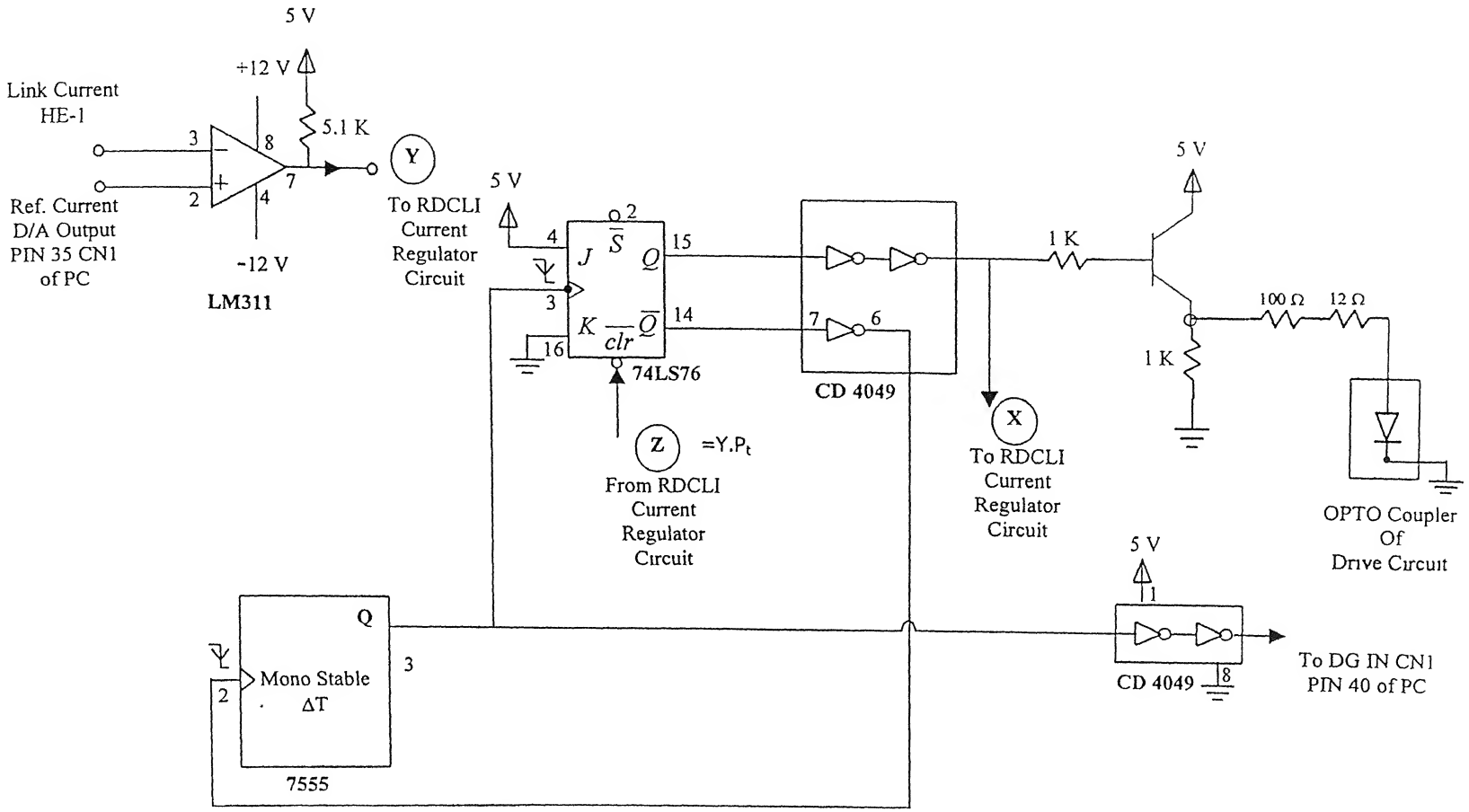


Fig. 6.5 Resonant dc link control circuit

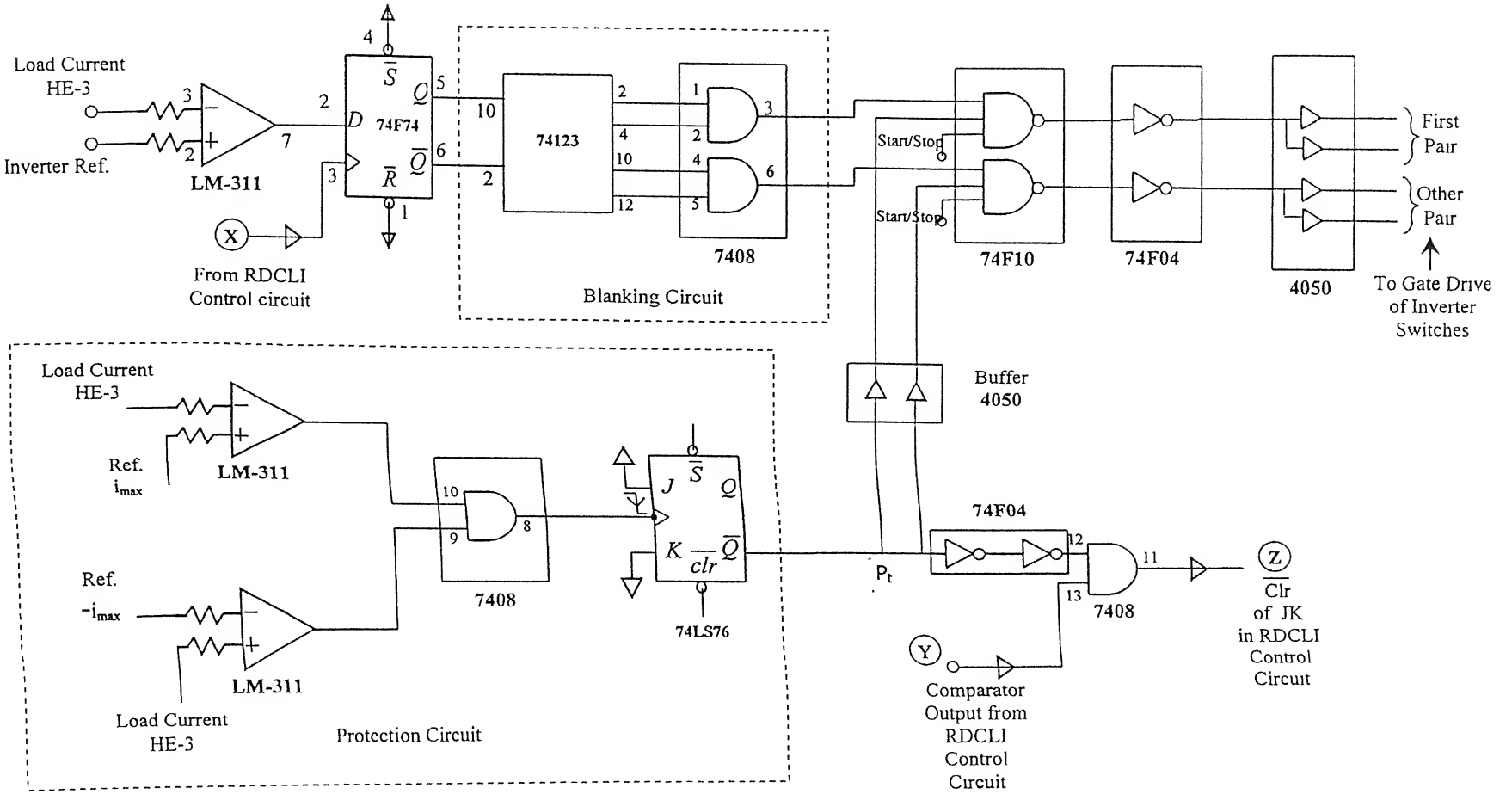


Fig. 6.6 RDCLI current regulator circuit

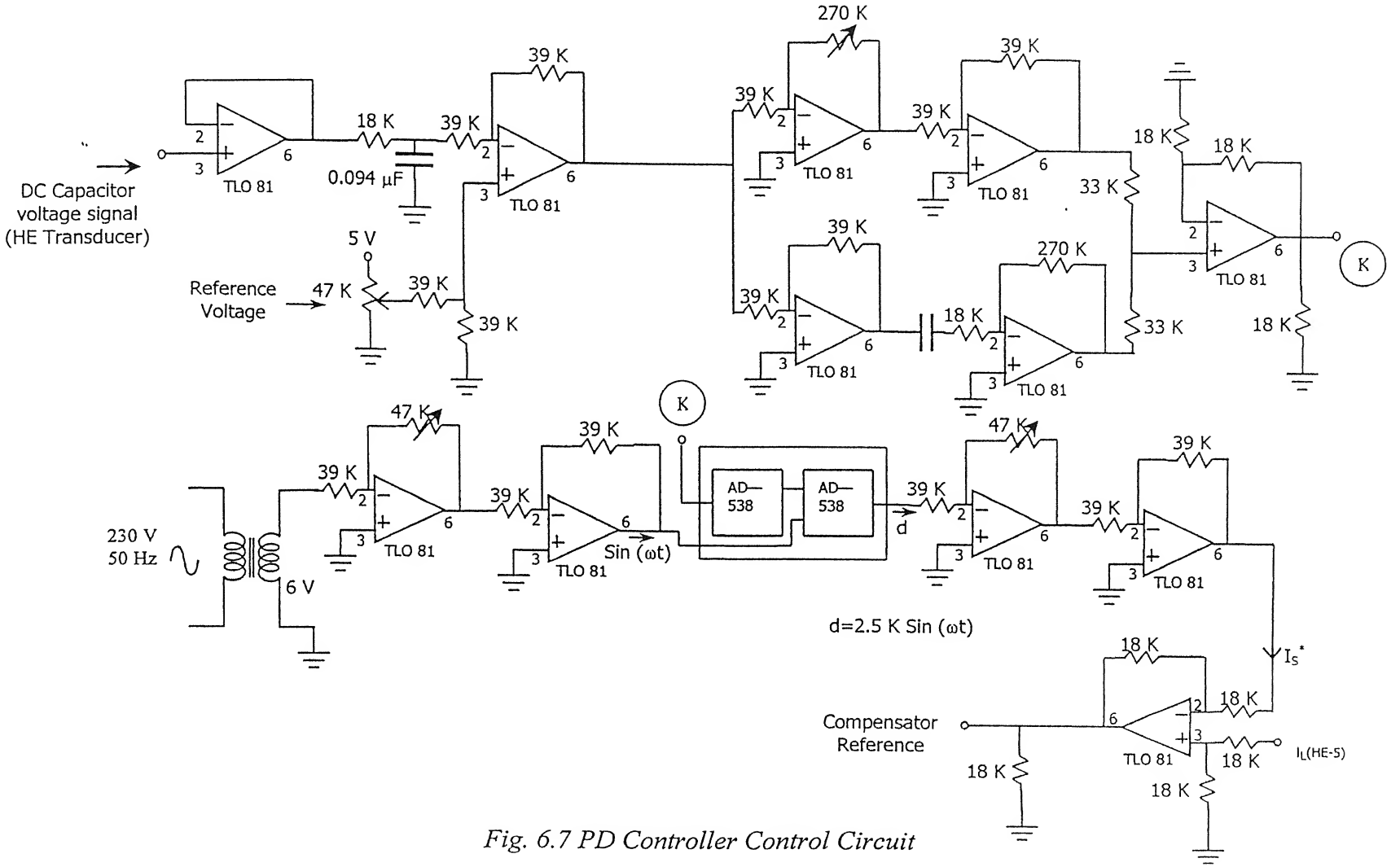


Fig. 6.7 PD Controller Control Circuit

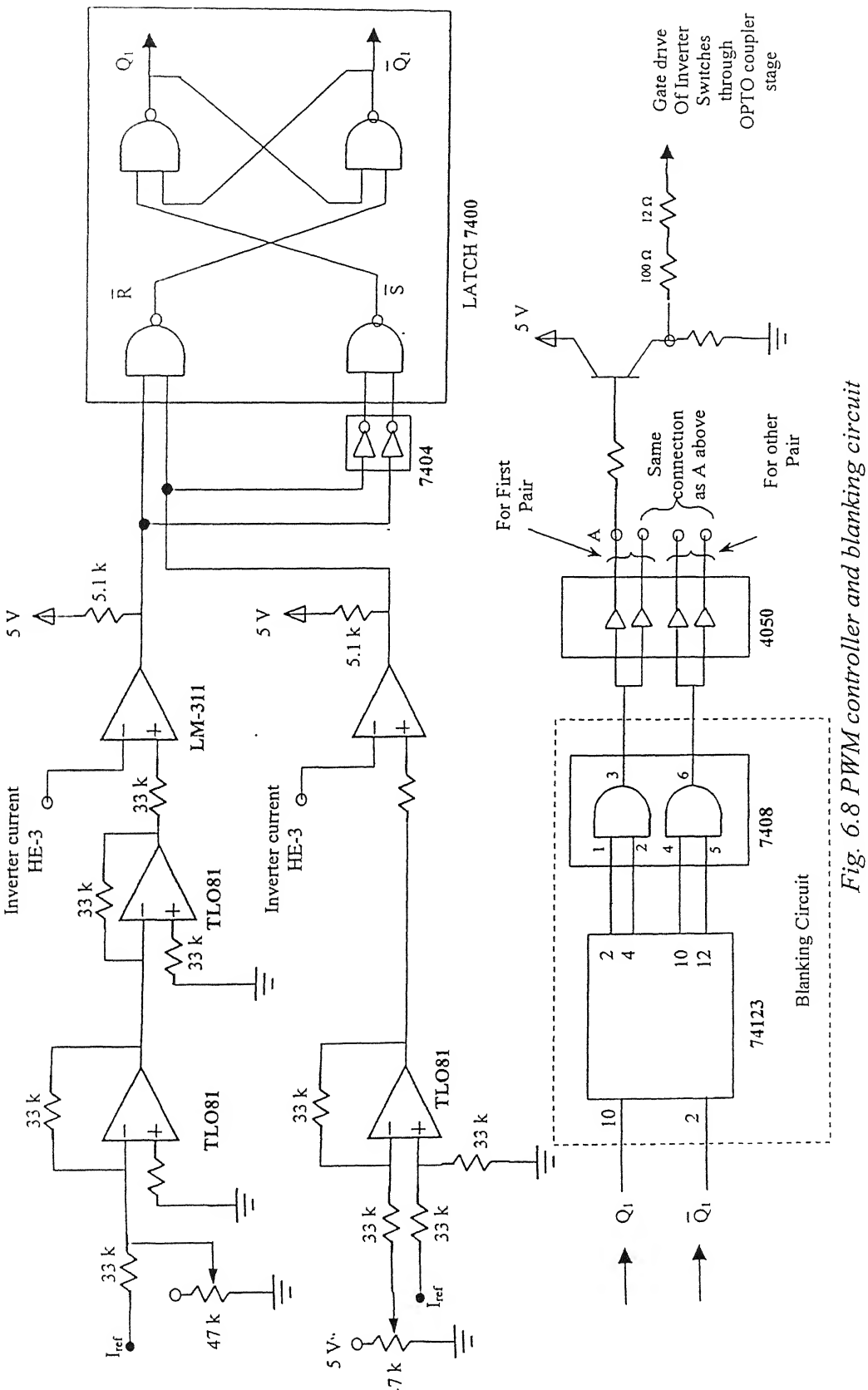


Fig. 6.8 PWM controller and blanking circuit

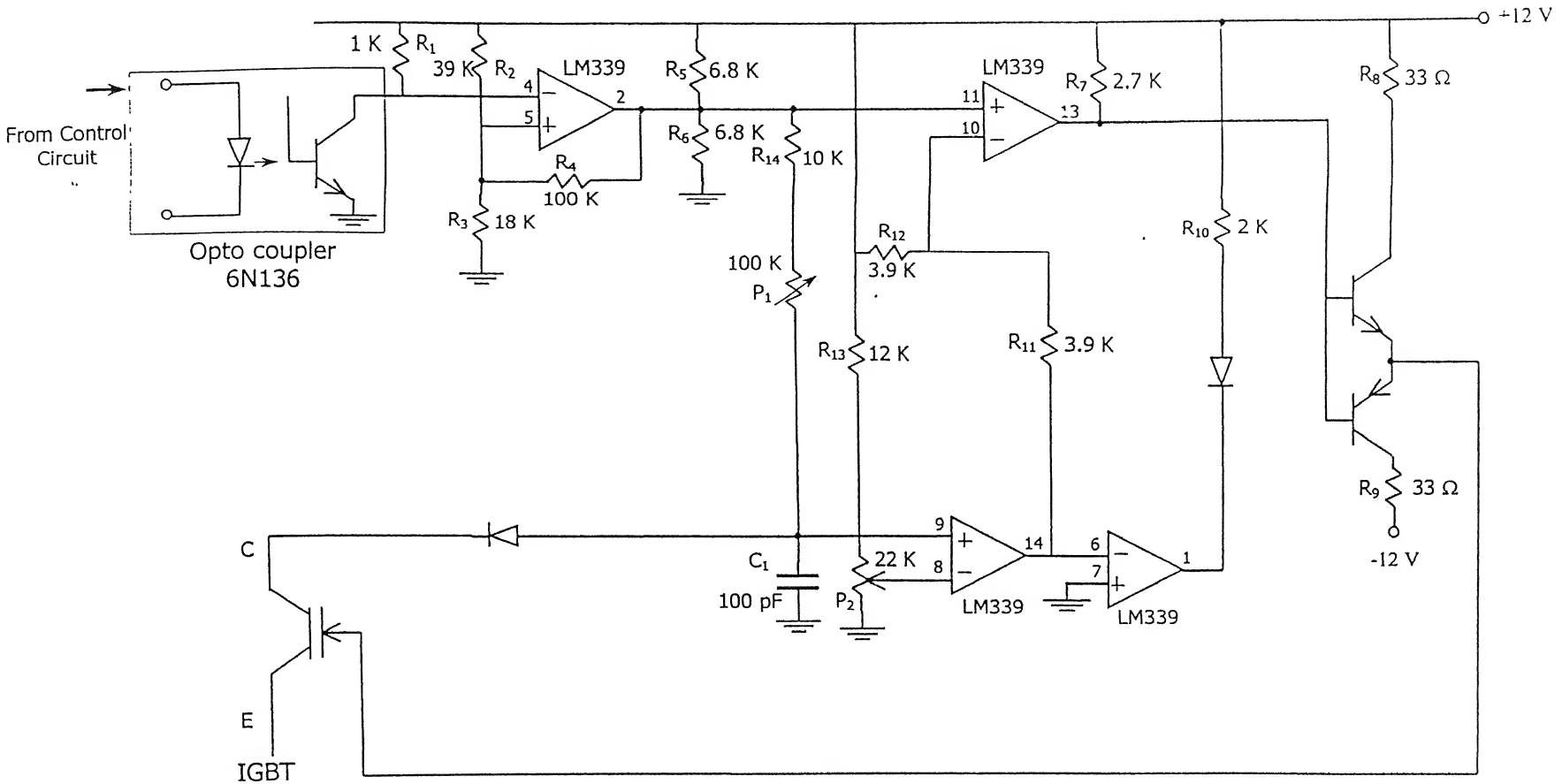


Fig. 6.9 IGBT gate drive circuit

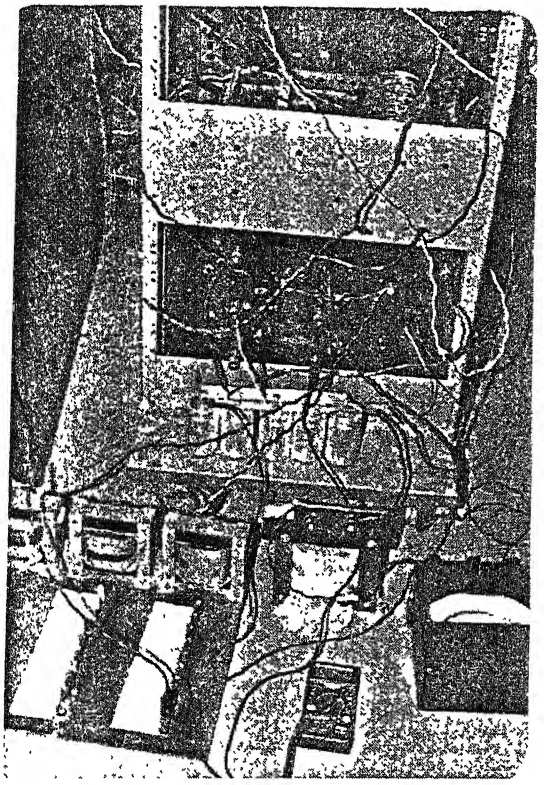


Fig. 6.10 Photograph of the power circuit displaying diode-bridge, filter inductor and capacitor

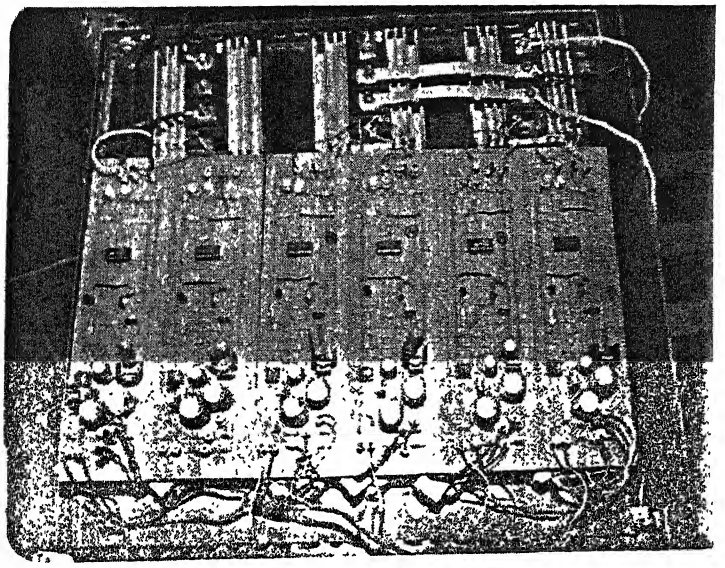


Fig. 6.11 Photograph of gate drive circuit and the IGBTs.

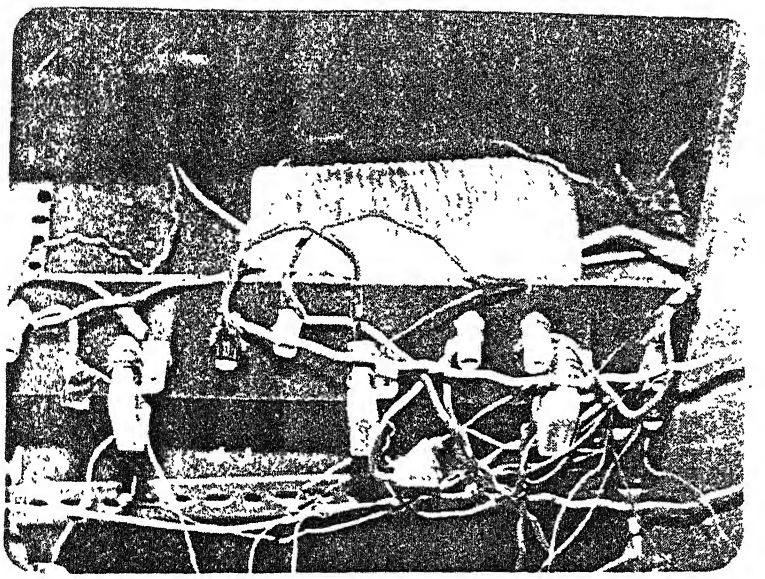


Fig. 6.12 Photograph displaying litz-wire inductor and current transducers

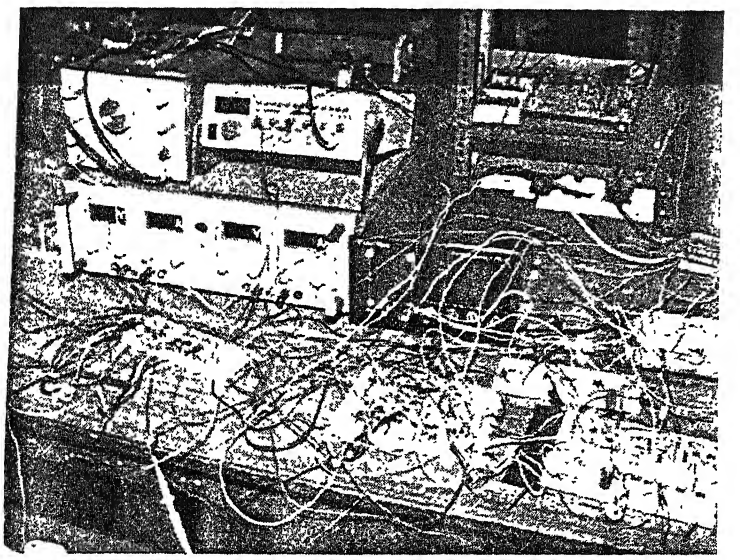


Fig. 6.13 Photograph displaying various control circuits, instruments and side view of power circuit

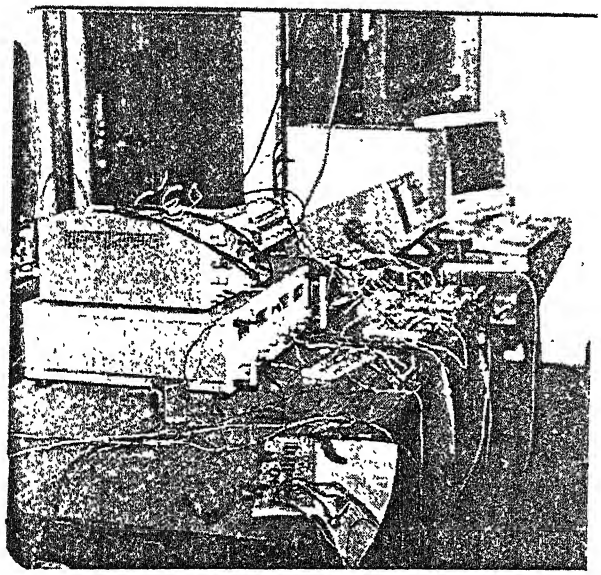


Fig. 6.14 Photograph displaying various control circuits and PC interface

CHAPTER 7

EXPERIMENTAL RESULTS

In this chapter the experimental results obtained in the laboratory are presented. For these results we have considered both RDCLI and PWM inverter based single-phase AHCC. The experiments are conducted at a lower power level since the objective is to verify the principles already discussed in earlier chapters. We start our discussions with the current initialization.

7.1 CURRENT INITIALIZATION

For the experimental set-up the resonant link parameters chosen are:

- $L = 52\ \mu H$
- $C = 0.89\ \mu F$
- $Q = 60$
- $V_{dc} = 65$ V (constant)

With these values of inductor and capacitor the link frequency is 23.4 kHz and resonant time is about 42.75 μs. Therefore, time duration of 37.5 μs is chosen as the resonant cycle time ΔT taking account of the finite Q-factor of the coil.

The block diagram of the current initialization scheme is shown in Fig. 3.5. Through this scheme, the zero-voltage switching (ZVS) is obtained. First, this ZVS property of the inverter is tested with no load conditions ($i_0 = 0$). This is to test whether the link voltage goes to zero after every 37.5 μs.

The experimental results with no load are shown in Figs. 7.1 to 7.3. In Fig. 7.1, the link voltage, link current and the gating signal of switch S_0 are shown. The link voltage

goes to zero after 37.5 μs after the prescribed time (ΔT). The switch S_0 is then turned on as is evident in Fig. 7.1. This switch remains in on state for time Δt so that the link current builds up to the desired level. During this shorting interval, the link current increases linearly which can be seen from this figure. The link current and the output of the monostable are shown in Fig. 7.2. From this figure it can clearly be seen that the monostable goes low after about every 37.5 μs and remains low in that state till the comparator is activated. When the comparator output goes low, the monostable is triggered. This remains high for 37.5 μs after which it goes low. In the meanwhile the comparator is reset. The required value of current for initialization is given to the comparator. When the actual link current is equal to this value, comparator output goes low again and the resonant cycle restarts. This is illustrated in Fig. 7.3. Thus Figs. 7.1 to 7.3 clearly illustrate the principle of working of the proposed current initialization for the RDLCI. Current initialization at a constant load current (2 A) is shown in Fig. 7.4. The constant current is achieved by putting a large inductance and a resistor at the output of the link. The level to which the current should be initialized is changed which is evident from this figure. The amount of change in initial value of link current is approximately equal to the load current.

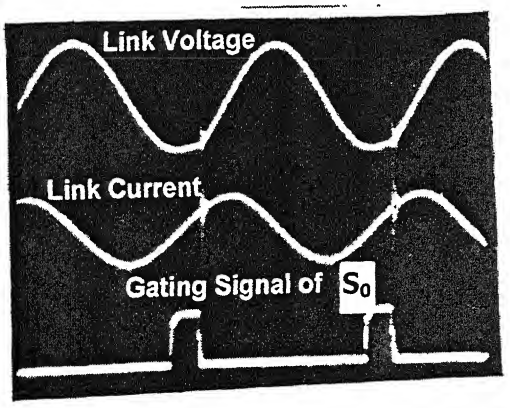
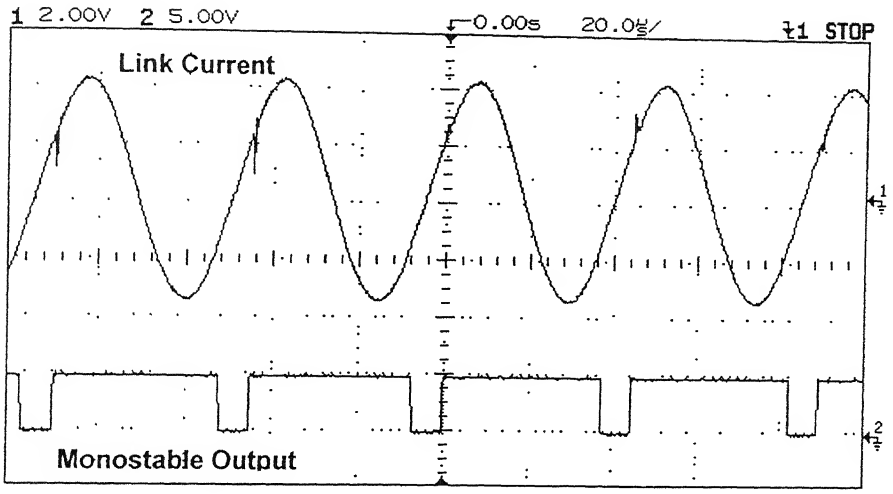


Fig. 7.1 Link voltage, link current and gating signal under no load conditions

Comparing Figs. 7.2 and 7.4 we can see that for zero load current, the average link current is little higher than zero. This average current has a distinct positive dc bias when the RDCLI is required to supply a load current of 2 A. Furthermore, the link current is initialized to 4.4 A when the load current is zero, and it goes up to about 6.4 A when the link supplies a constant load current of 2 A.



Channel-1: 1 V corresponds to 2.22 A

Fig. 7.2 Link current and monostable output

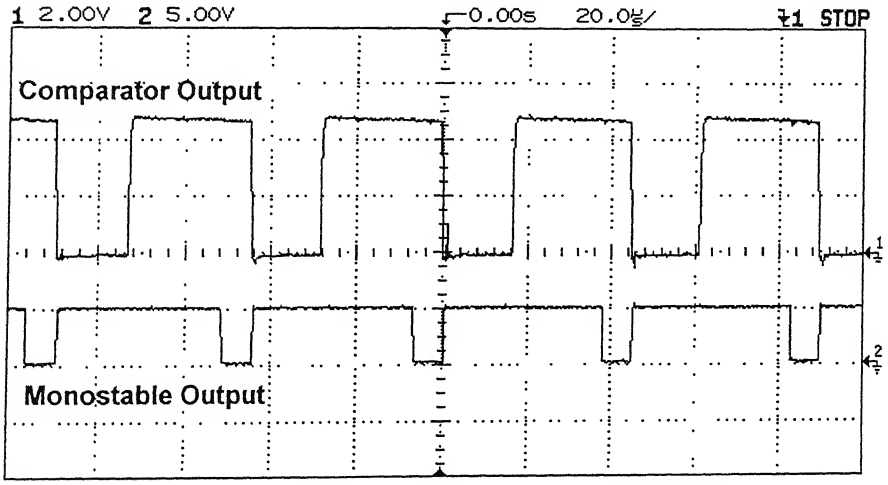
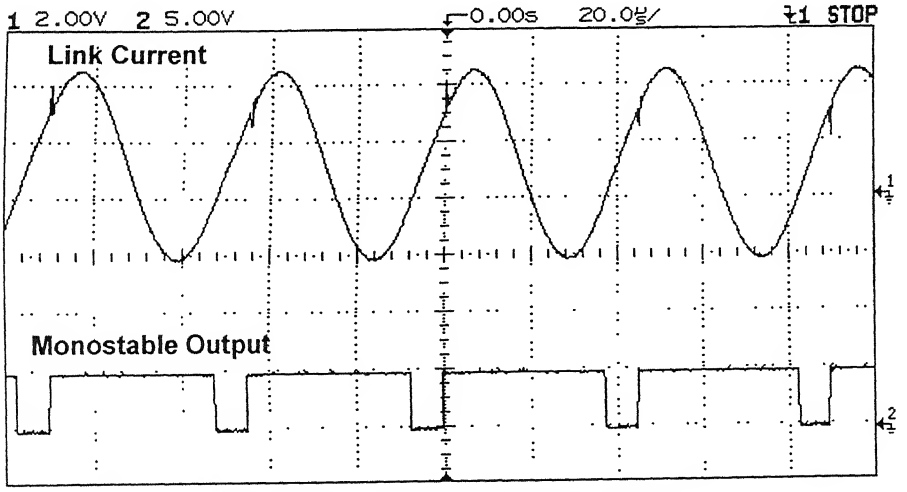


Fig. 7.3 Comparator output and monostable output



Channel-1: 1 V corresponds to 2.22 A

Fig. 7.4 Current initialization at constant load current

We also carry out simulation studies with the same parameters as used in the experimental setup. The link voltage goes to zero after every 37.5 μs as evident from the simulation results shown in Fig. 7.5 and 7.6. It can be seen that the link capacitor voltage has a peak of about 130 V and the current rises linearly during Δt. The value to which the current is built up, is 4.4A for zero load current and 6.4A for constant load current of 2A. The experimental results are in close agreement with the simulation results.

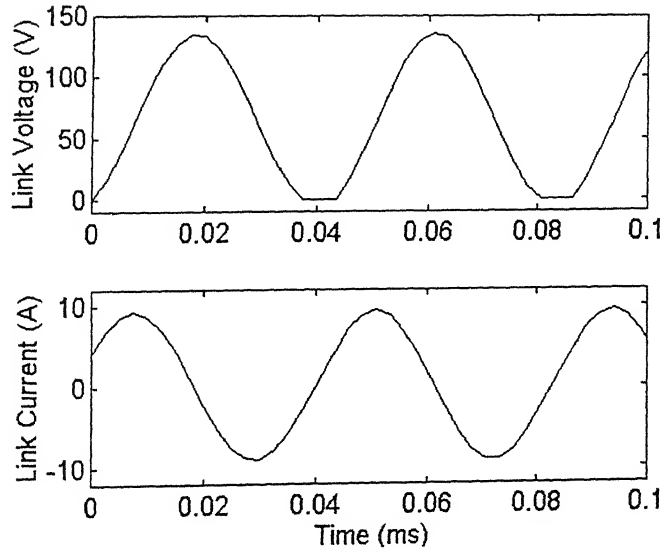


Fig. 7.5 Link voltage and link current waveform for zero load current

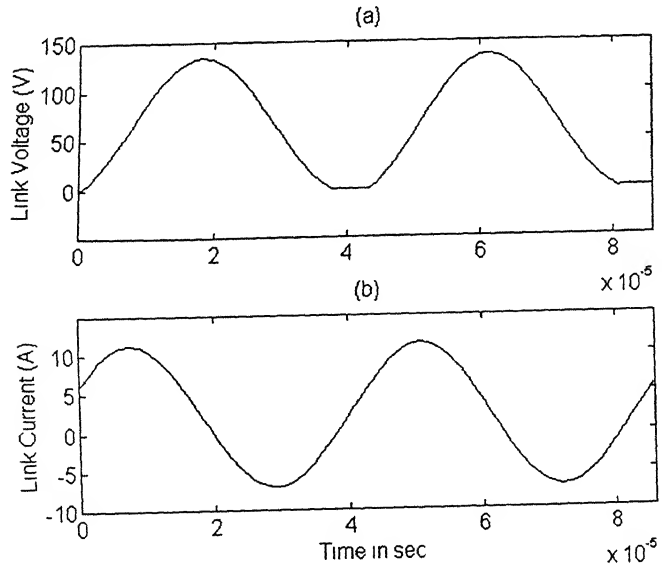


Fig. 7.6 Link voltage and link current waveform at constant load current of 2A

7.2 FREQUENCY RESPONSE TEST

A RDCLI is normally used for motor drive application. It can further be used for active filtering [24], sophisticated power supplies. It is therefore important to show the capability of this device to track reference waveforms of different nature, amplitude and frequency. Consider the schematic diagram shown in Fig. 7.7. The purpose of this test is to demonstrate this behavior. In this test, a reference current is generated from a signal generator. The inverter is constrained to follow this reference current in a zero hysteresis bang-bang mode by properly gating the switches $S_1 - S_4$. The load in Fig. 7.7 chosen for this study contains an inductance of 17 mH and a resistance of 10 Ω.

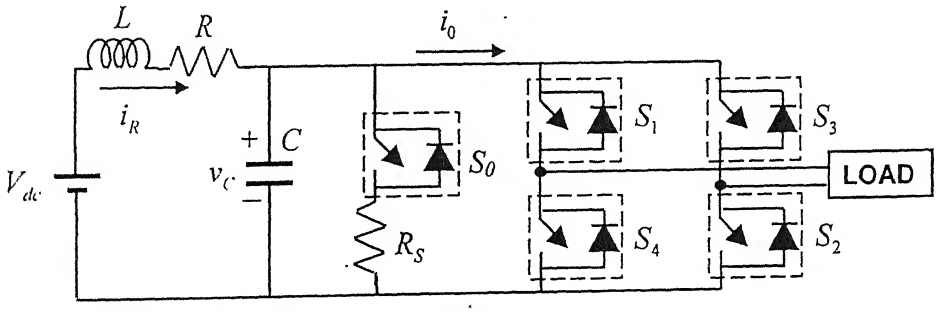


Fig. 7.7 Set-up for resonant link supplying a specific load

In the first instance, a sinusoidal reference current of amplitude 1 A and frequency 100 Hz is chosen. The simulation and practical implementation results, which are in close agreement, are shown in Fig. 7.8 and 7.9 respectively. It can be seen that the inverter properly tracks the reference current. However the actual inverter current contains high frequency ripple due to high frequency switching. For this test the current i_0 (see Fig. 7.7) is a variable that takes on different positive and negative values in a continuously variable form in order to track the reference current. However, ZVS is achieved for all load currents. It has been observed experimentally that the zero voltage switching is maintained under this condition of varying load current.

Further to illustrate this principle, a triangular reference current of magnitude 2 A and frequency 100 Hz is chosen. The reference and tracking waveforms for the practical implementation are shown in Fig. 7.10. It can be seen that the reference is tracked

perfectly. We have also conducted frequency response tests up to 1 kHz. These results are quite satisfactory. It is however to be noted that the success of the test will depend on the quality of the load inductor. If it saturates at higher frequency and voltage level, the tracking will be inferior.

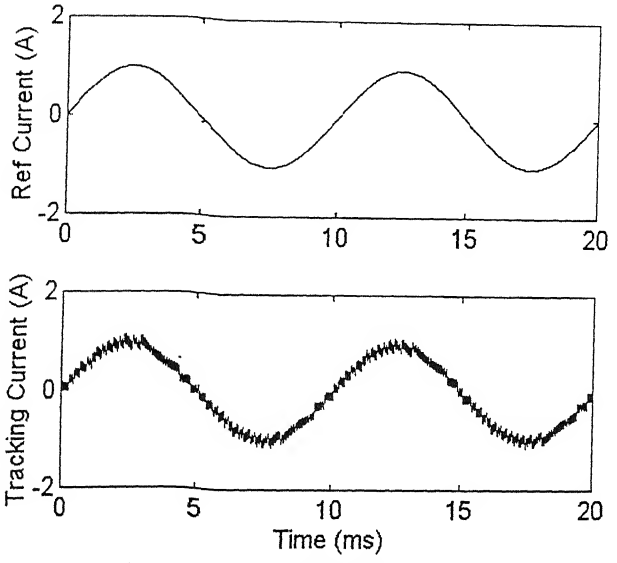


Fig. 7.8 Tracking of 100 Hz sinusoidal signal (Simulation result)

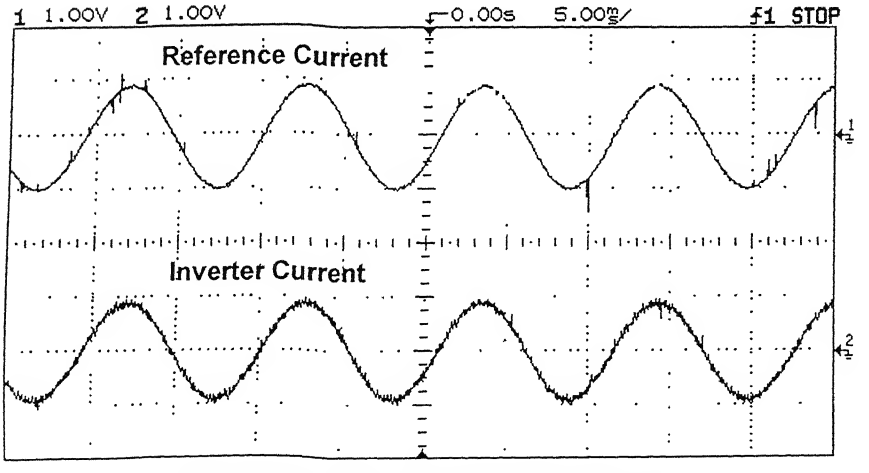


Fig 7.9 Tracking of a 100 Hz sinusoidal signal (experimental result)

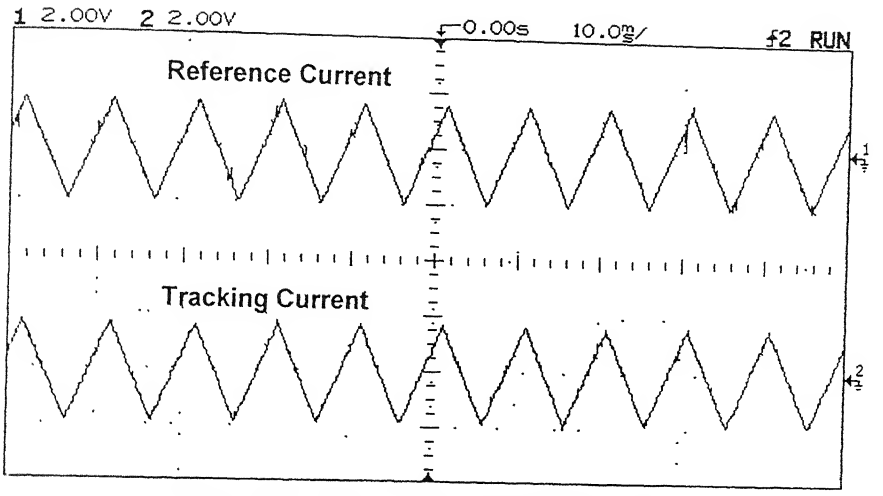


Fig. 7.10 Tracking of a 100 Hz triangular wave

7.3 RDCLI AS LOAD COMPENSATOR

In this test, the RDCLI is used for power factor correction. This is illustrated in Fig. 7.8 in which an R-L load is connected to an ac supply voltage v_S. It is well know that the source current (i_S) will lag the supply voltage. We now inject a current (i_F) through the RDCLI such that the source current (i_S) is in phase with v_S. This is done at the point of common coupling p at which the output current (i_F) is injected into the network through an interfacing inductor (L_F). In this example we have chosen the following:

Ac supply voltage v_S: $50\sin(100\pi t)$

Load inductance L_L: 275.7 mH

Load resistance R_L: 50 Ω

Interface inductance L_F: 17 mH

First we measure the load current when the RDCLI is not connected at the point of common coupling. This current is found to have a peak value of 0.5 A and has a phase angle of 60° (lagging) with respect to the source voltage. Therefore the active component of this current has a peak value of 0.25 A. Applying KCL at the point of common coupling p, we set a reference for the RDCLI current (i_F) as $i_l - 0.25\sin(100\pi t)$, where i_L is measured using a Hall-effect current sensor and the second component is phase-locked with the supply voltage. It may be noted that this is

an example. We demonstrate that RDCLI can supply such a current so that a unity power factor of the source current can be achieved.

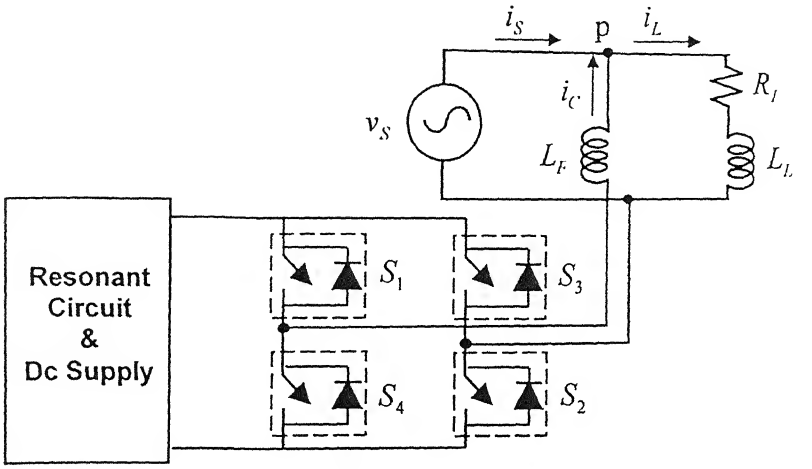


Fig. 7.11 Set-up for RDCLI based load compensator

The simulation results for this case are shown in Fig. 7.12 in which the source voltage is scaled down by a factor of 50 such that its amplitude is comparable to that of the current. The experimental results are shown in Fig, 7,13and 7.14. It is evident from these figures that the simulation and experimental results are in close agreement. Furthermore, in both these cases, the RDCLI tracks the reference current properly thereby forcing the source power factor to be unity.

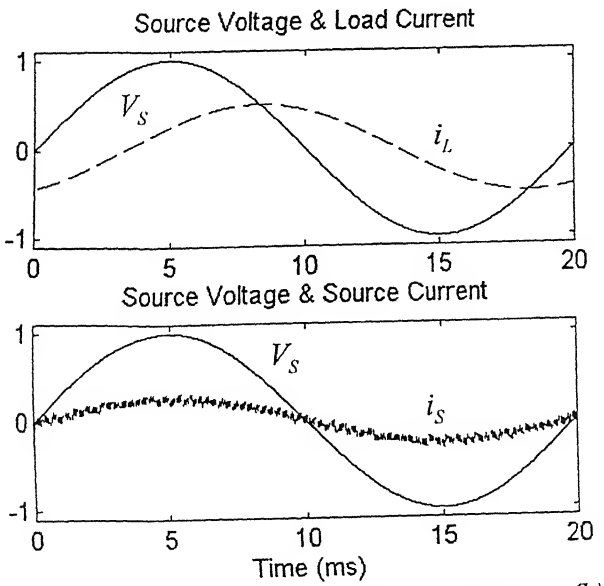


Fig. 7.12(a) Waveform of supply voltage and load current; (b) Waveform of supply voltage and source current.

- PD Controller: $K_p = 0.9, K_D = 0.4, N = 20.$

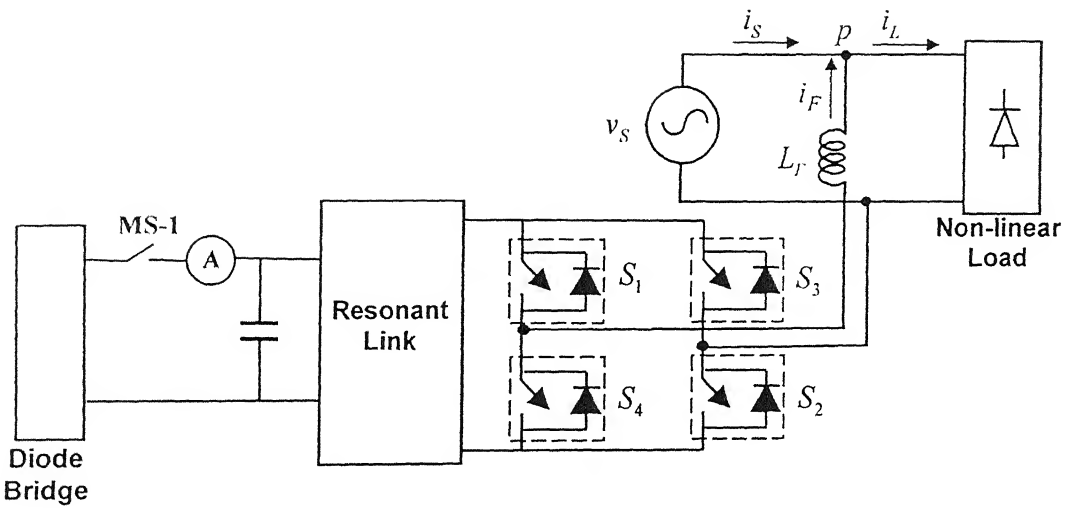


Fig. 7.15 Schematic of RDCLI based AHCC

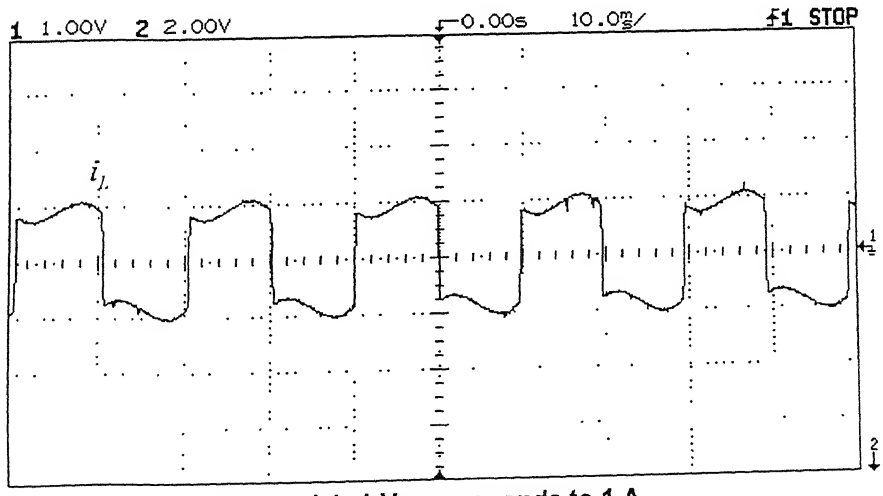
It is to be noted that for the earlier experiments the RDCLI was supplied by a dc source. For this experiment it is important that the capacitor voltage is maintained by the PD controller. However, for start up we charge the dc capacitor through a diode-bridge such that the resonance of the link is sustained. Once the link stabilizes, we switch on the PD controller. Once the controller takes over the operation of the circuit, the mechanical switch MS-1 of Fig. 7.15 is turned off. Furthermore to measure the current drawn by the dc capacitor from the diode-bridge we also have connected an ammeter in series with the mechanical switch. It is interesting to note to once the PD controller takes over, this ammeter reads zero to indicate that no power is drawn from the diode-bridge (charging circuit). The switch MS-1 is turned off at this point. Tests with the following two different non-linear loads are performed.

- Diode-bridge with RL load at its output terminal
- Diode-bridge with RC load at its output terminal (switch-mode power supply type)

These tests are discussed below.

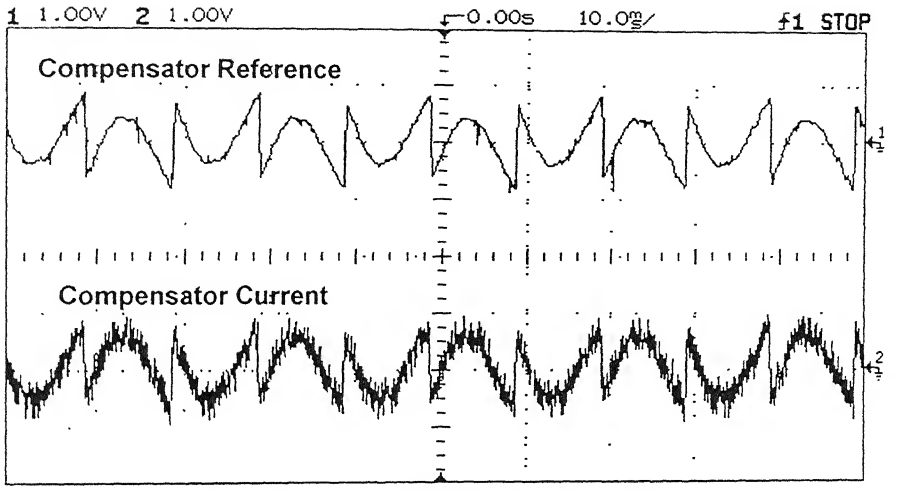
7.4.1 Diode-bridge with RL at its Output Terminal

The source supplies a diode-bridge that has a large inductor and a resistor connected to its output. The values of the inductor and resistor are chosen such that the output current of the diode bridge is 1 A. The current that the diode-bridge draws from the source is of the shape as shown in Fig. 7.16. This is the load current i_L that will be drawn from the source in the absence of the compensator. Now the compensator is connected such that it injects a current at the point of common coupling. The compensator reference is obtained from the PD controller card given in Fig. 6.6 and discussed in Section. 6.4. The inverter is subjected to supply this current. The reference current and compensator current are shown in Fig. 7.17. It is clear from this figure that the inverter tracks this fast varying current very accurately. The compensated source current is shown in Fig. 7.18. This current is shown along with the source voltage (scaled down by a factor of 40) to show the power factor correction property of this AHCC. The dc capacitor voltage is shown in Fig. 7.19. It is observed that this voltage is held constant at a steady state value 67.5 V.



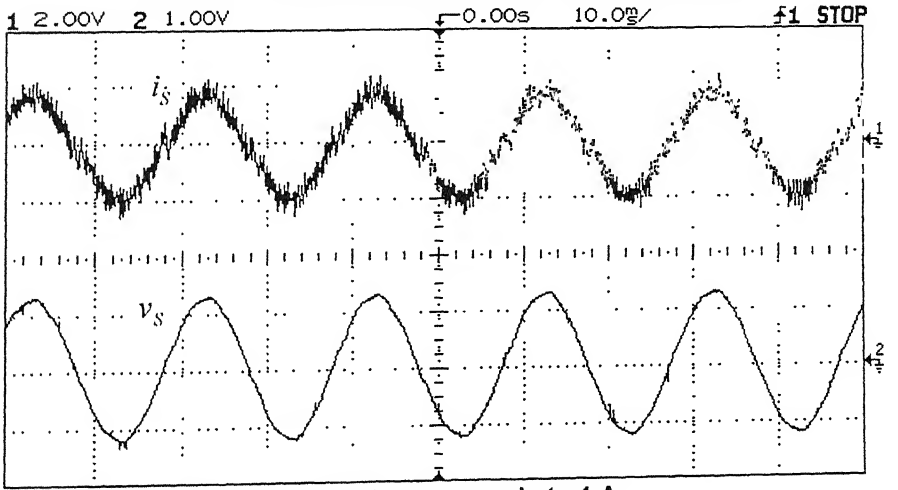
Channel-1: 1 V corresponds to 1 A

Fig. 7.16 Waveform of the load current



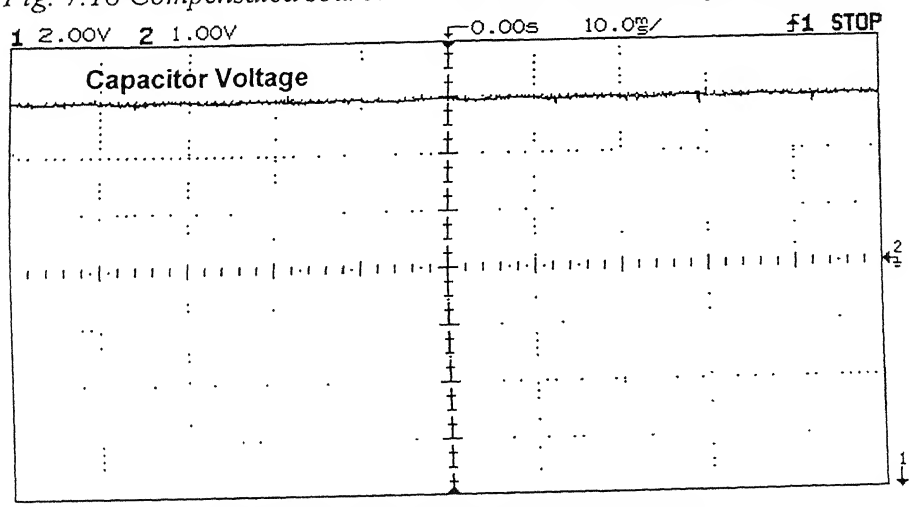
Channel-1 & 2: 1 V corresponds to 1 A

Fig. 7.17 Compensator reference and its tracking



Channel 1: 1 V corresponds to 1 A
Channel 2: 1V corresponds to 1V

Fig. 7.18 Compensated source current and source voltage waveform



Channel 2: 1V corresponds to 22.2 Volts

Fig 7.19 DC capacitor voltage waveform

7.4.2 Diode-bridge with RC at its Output Terminal

Next we consider a diode-bridge with capacitor at its output terminal. This load is essentially similar to that of a switch-mode power supply (SMPS). The current drawn is concentrated into a short burst of about 2-3 ms for each half cycle. The compensator reference and its tracking are shown in Fig. 7.20, while Fig. 7.21 shows the compensated source current along with the compensator and load currents. It is clear that the compensator faithfully tracks the reference current thereby making the source current sinusoidal.

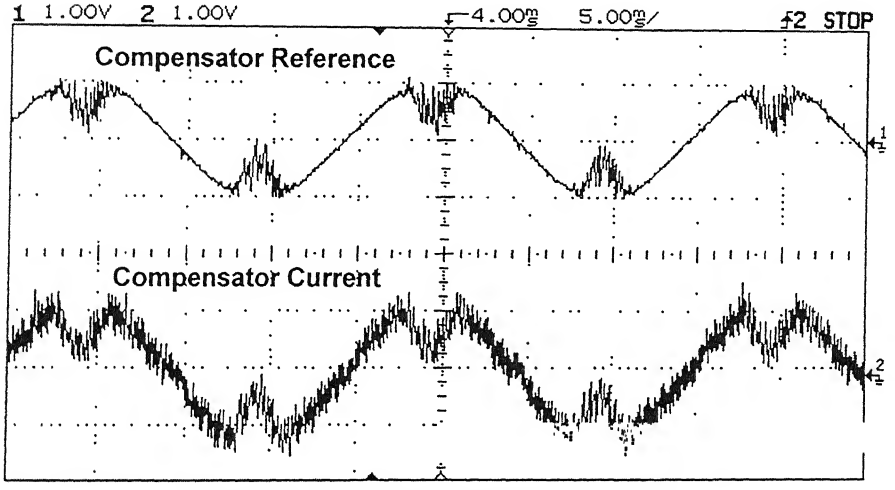


Fig. 7.20 Compensator reference and its tracking under SMPS type load

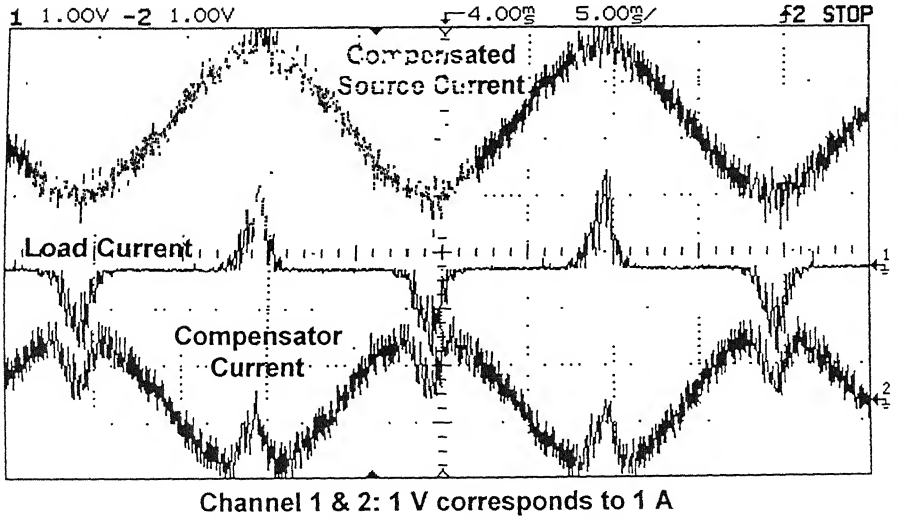
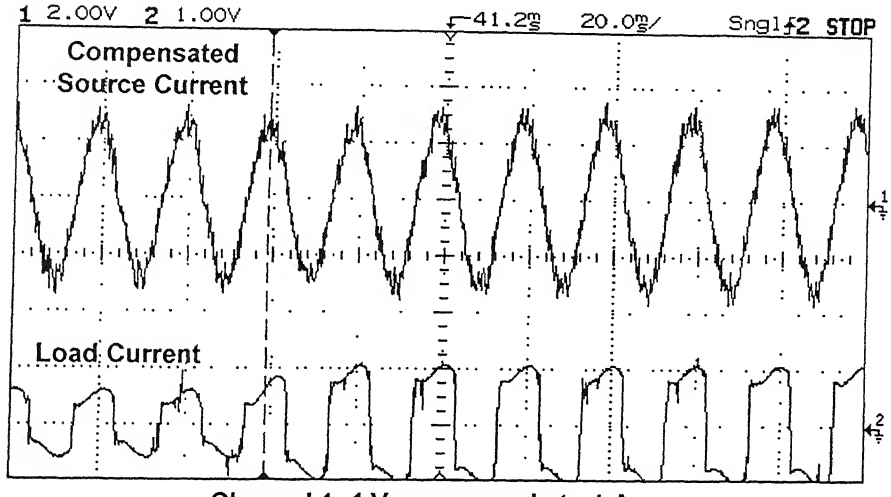


Fig 7 21 Load current, compensator current and compensated source current with SMPS type load

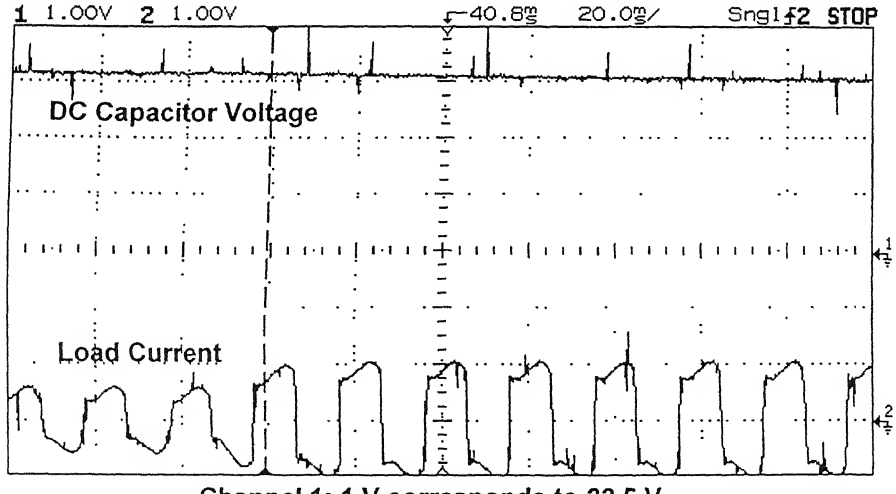
7.4.3 Transient Response of PD Controller

In this section the transient response of the compensator in conjunction with the PD controller is presented. The load considered for this case is a diode-bridge with RL at its output. The load draws a steady state current of 0.6 A when it is suddenly increased to 1 A. The source current settles to its new value in about 3 cycles. This is shown in Fig. 7.22. The capacitor voltage change in transient condition is shown in Fig. 7.23. The change in the error in capacitor voltage is shown in Fig. 7.24. In all these cases it is clear that the settling time of the compensator is about 3 cycles.



Channel 1: 1 V corresponds to 1 A
Channel 2: 1V corresponds to 1 A

Fig. 7.22 Load current and compensated source current in transient conditions



Channel 1: 1 V corresponds to 22.5 V
Channel 2: 1V corresponds to 1 A

Fig. 7.23 Load current and dc capacitor voltage in transient conditions

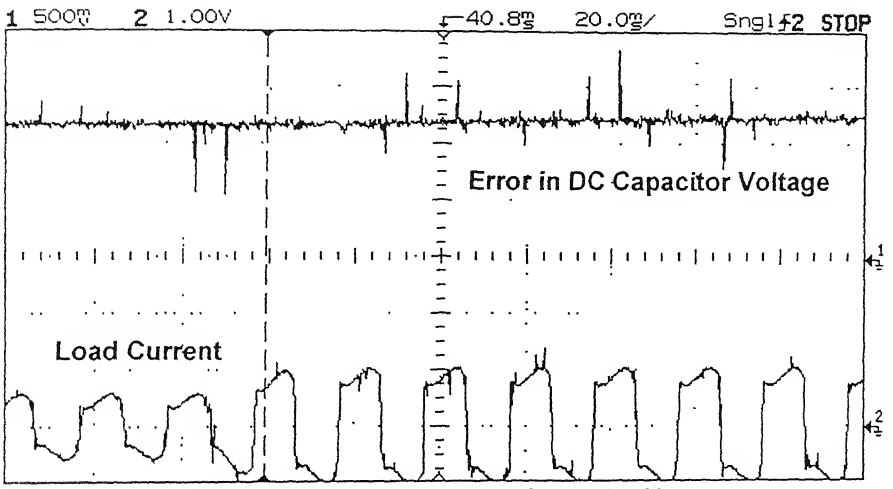


Fig. 7.24 Load current and error in dc capacitor voltage in transient conditions

7.4.4 Losses in RDCLI based AHCC

We now want to investigate the losses incurred using RDCLI based AHCC, especially the effect of the dc capacitor voltage on the losses. To do that we connect the same diode-bridge as load and put an ac wattmeter on the source side (i.e., to the left of point *p*, point of common coupling in Fig. 7.15). This implies that the wattmeter will indicate the power drawn from the source. The average power drawn from the source for various values of dc capacitor voltage and load current are shown in Table. 7.1. The second column of the table gives the losses in the system when the load is disconnected from the supply (i.e., the load current is zero). This implies that the values indicated in this column are purely the losses supplied by the source to the compensator circuit. It is however to be noted that the loss in the compensator circuit is the sum total of inverter switching loss, I^2R loss due to finite Q factor of interface inductor, losses in the resonant link, losses in the energy storing capacitor and losses in the connecting wires.

We can then conclude from the first two columns of Table. 7.1 that losses in the compensator circuit increase with the increase in dc capacitor voltage. The same can also be concluded from the 3rd and 4th column of this table which lists the power drawn

from the source when the load current is 0.7 A and 1.1 A respectively. It is well known that the power consumed by a diode-bridge is given by

$$P_{diode} = \frac{2E_m}{\pi} I_d \tag{7.1}$$

where E_m is the peak value of the voltage applied across it (50 V for our experiment) and I_d is the current at the output of the diode-bridge. The load current i_L is $2I_d$ peak-to-peak. Then the power consumed by the diode-bridge is 22.28 W and 35 W for load currents of 0.7A and 1.1A respectively. We must also add the loss in the diode-bridge with it. Comparing the figures given in each corresponding of Table. 7.1 we can say the loss in the diode bridge is roughly 5 W. However, since the power drawn by the diode-bridge and its losses are (almost) independent of the dc capacitor voltage, the increase in the power supplied by the source with V_{dc} in 3rd and 4th column are also indicative of the increased losses in the AHCC circuit. The results given in Table 7.1 are graphically shown in Fig. 7.5.

It is therefore important to run the link at a voltage level that is just sufficient to force current at a desired rate through the interface inductor. Otherwise the losses in the circuit will increase. The choice of the interface inductor is also very crucial for the same reason. A smaller inductor will enable the link to operate at a relatively lower dc voltage at the cost of chattering in the compensator current. Furthermore, the isolation in this case will also degrade. On the hand, a large value of inductor will make it difficult for the RDCLI to force current at a desired rate without raising the dc voltage. A judicious choice of the values of L_F and V_{dc} are therefore recommended.

Table 7.1 Power drawn from source for various load currents and dc voltages

V_{dc} (V)	Power drawn from source for different load currents		
	0 A	0.7 A	1.1 A
65	25 W	52 W	65 W
68	27 W	54 W	67 W
70	31 W	56 W	69 W
72	33 W	59 W	73 W
75	35 W	60 W	75 W

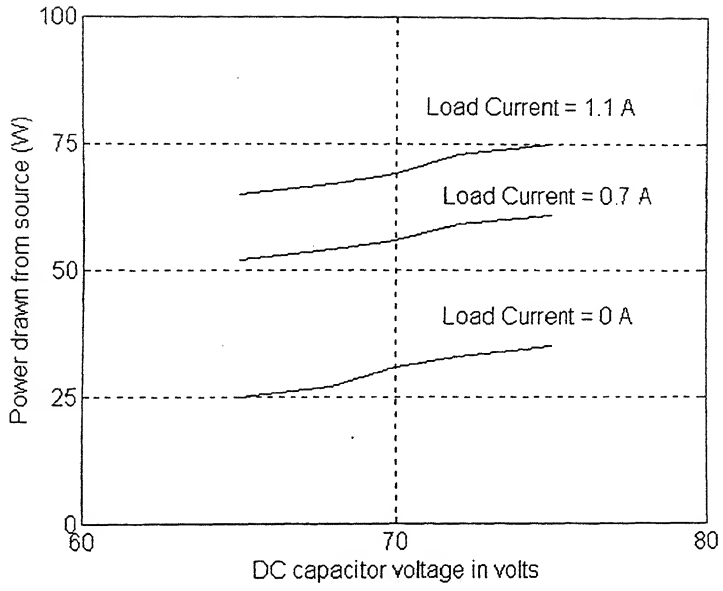


Fig. 7.25 Power drawn from source at different values of dc capacitor voltage and different load currents

It is observed that with a PD controller the dc capacitor voltage assumes different steady state values at different values of load currents. This fact is also depicted in Fig. 7. 23 and 7.24. However, the AHCC system performance is not affected by this steady state error. This is because the dc capacitor voltage is maintained at a value still higher than the peak value of the ac supply voltage. However the steady state error when a PI controller is used in place of a PD controller. For the purpose of comparison we also employ a PI controller. This controller is of the form

$$G_c(s) = \frac{0.12s}{1+0.02s} \tag{7.2}$$

The all other parameters in the system remain unchanged and the performance of the AHCC with PI controller is evaluated with the same diode-bridge with RL load at its output. The different steady state capacitor voltage values are given in Table. 7.2 for different values of load currents with PD and PI controllers. The results are also depicted graphically in Fig. 7.26.

However, as discussed earlier a higher value of dc capacitor voltage would result in higher losses in the AHCC. Therefore for the same value of load current the AHCC would incur more losses when operated with a PI controller compared to that of a PD

controller. Table. 7.3 represents the power drawn from source at different load currents for PD and PI controller corresponding to dc voltages given in Table. 7.2. It is to be noted that the diode-bridge would draw a particular amount of power for a specific load. As discussed earlier the total power includes the load power and the losses in the AHCC. Therefore at a specific value of load current a higher value of the power drawn from ac source implies higher losses in the AHCC. This is presented graphically in Fig. 7.27. From these figures it is evident that losses increases with the PI controller for the same load current.

Table 7.2 DC capacitor voltage with different load currents with PD & PI controller

i_L (A)	$V_{dc}(V)$	
	PD Controller	PI Controller
0	74	78
0.2	72	78
0.5	70	77.5
0.7	68	77
1.1	65	77

Table 7.3 Power drawn from source with different load currents with PD & PI controller

i_L (A)	Power drawn from source (W)	
	PD Controller	PI Controller
0	35	38
0.2	42	47
0.5	49	59
0.7	54	68
1.1	65	78

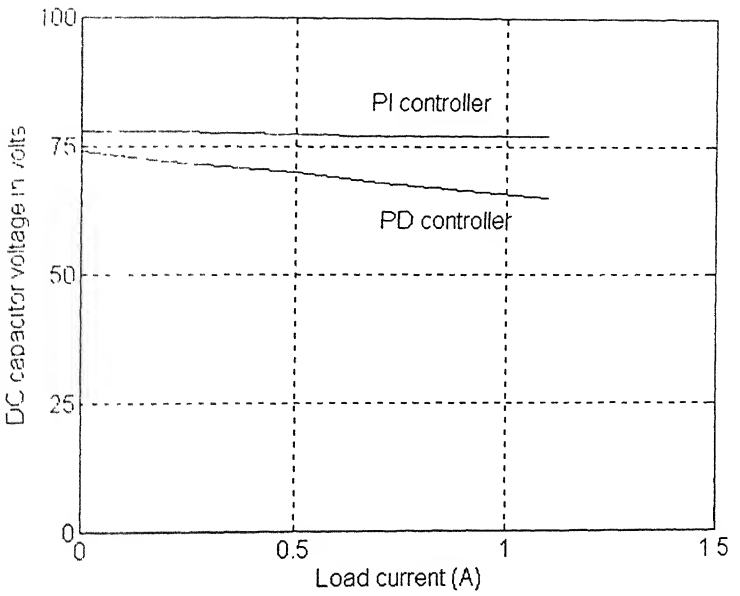


Fig. 7.26 Variation of dc capacitor voltage with load current with PD and PI controllers

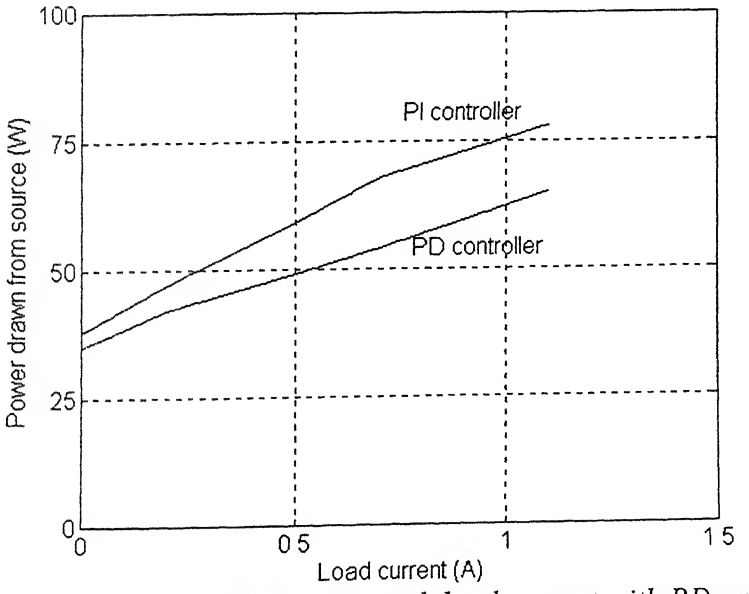
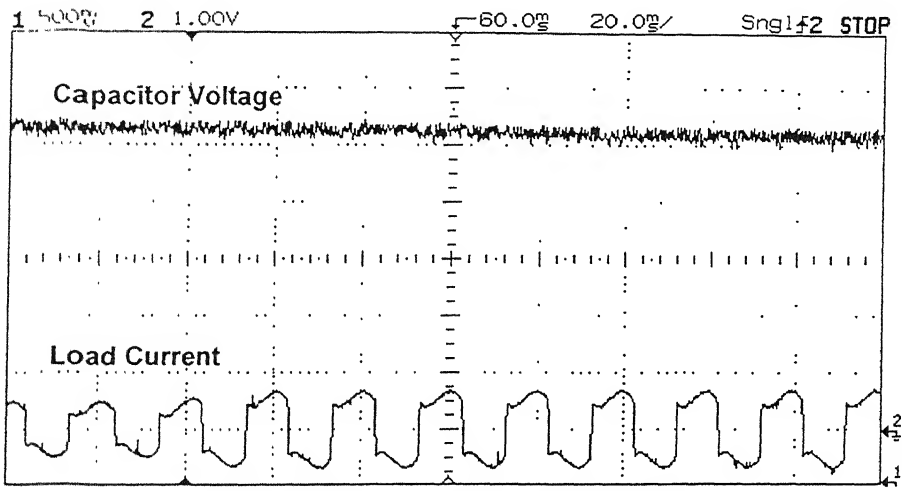


Fig. 7.27 Power drawn from source with load current with PD and PI controllers

7.4.5 Transient Response of the PI controller

We now investigate the transient response of the PI controller whose transfer function is given in Eq. 7.2. With the AHCC compensating a diode-bridge with RL load in steady

state, the load current is suddenly increased from 0.5 A to 0.8 A. With this load change there is also a change in the steady-state value of the dc capacitor voltage. This is shown in Fig. 7.28. Observing this figure minutely we can see that the dc capacitor voltage has not reached its steady state following the load change in 8 cycles. We can draw the same conclusion from Fig. 7.29, which depicts the compensated source current along with load current in transient. We can conclude that the PI controller has undesirably sluggish response compared to the PD controller.



Channel 1: 1 V corresponds to 22.2 V
Channel 2: 1 V corresponds to 1A

Fig. 7.28 DC capacitor voltage under transient conditions with PI controller

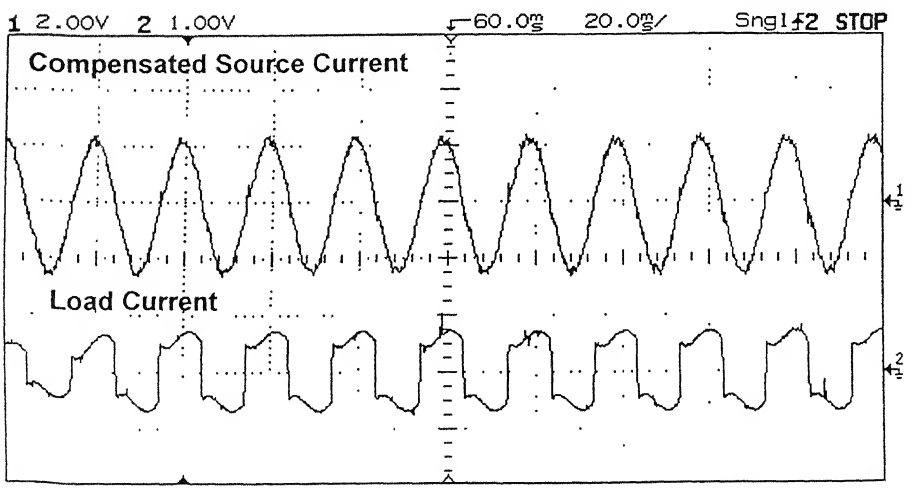


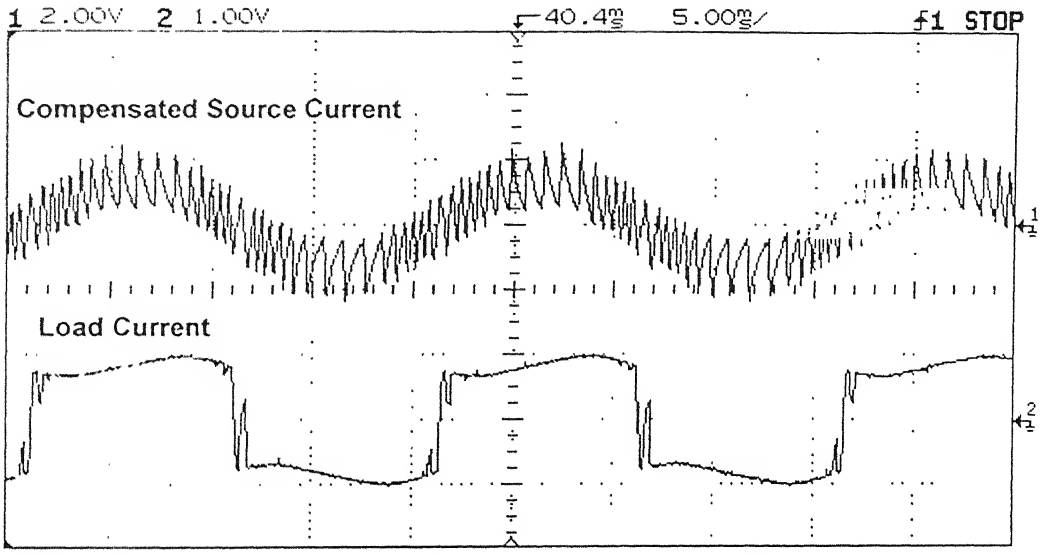
Fig. 7.29 Compensated source current and load current under transient conditions with PI controller

7.5 PWM INVERTER BASED AHCC

The experimental setup of this AHCC is shown in Fig. 6.2. The compensator reference is extracted from the PD controller card (Fig. 6.6) and the current control in the inverter is done using bang-bang current control. The parameters chosen for the experiment purpose are:

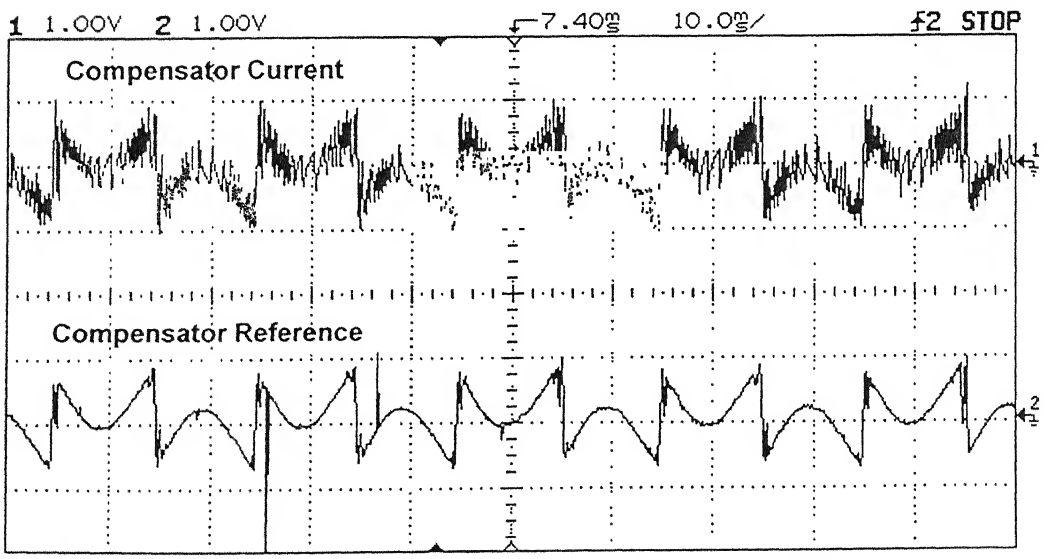
- Ac supply voltage v_s: $50\sin(100\pi t)$, Frequency 50 Hz.
- Load current 1 A
- Interface inductance L_f 3.85 mH
- Interface resistance R_f 0.5 Ω
- $K_p = 0.9$, $K_D = 0.4$, N 20.

The load is the diode-bridge with RL at its output. The load current and the compensated source current are shown in Fig. 7.30 for an average switching frequency of 1.65 kHz. It is seen that the ripple in the compensated current is large and hence the performance is not acceptable. Therefore the switching frequency is increased to 4.2 kHz by reducing the hysteresis band. The compensator reference and the tracking current are shown in Fig. 7.31. The compensated source current along with load current is shown in Fig. 7.32. We can see that the compensated source current is sinusoidal that has some high frequency ripple. However, comparing with Fig. 7.18 we can summarize that the ripple in this case has a significantly higher magnitude than with an RDCLI based AHCC. The ripple magnitude can further reduced by increasing the switching frequency. This will increase the system losses and device stresses.



Channel 1 & 2: 1 V corresponds to 1 A.

Fig. 7.30 Load current and compensated source current with PWM inverter based AHC'C at 1.65 kHz.



Channel 1 & 2: 1 V corresponds to 1 A.

Fig. 7.31 Compensator reference and actual compensator current with PWM inverter based AHC'C at 4.2 kHz.

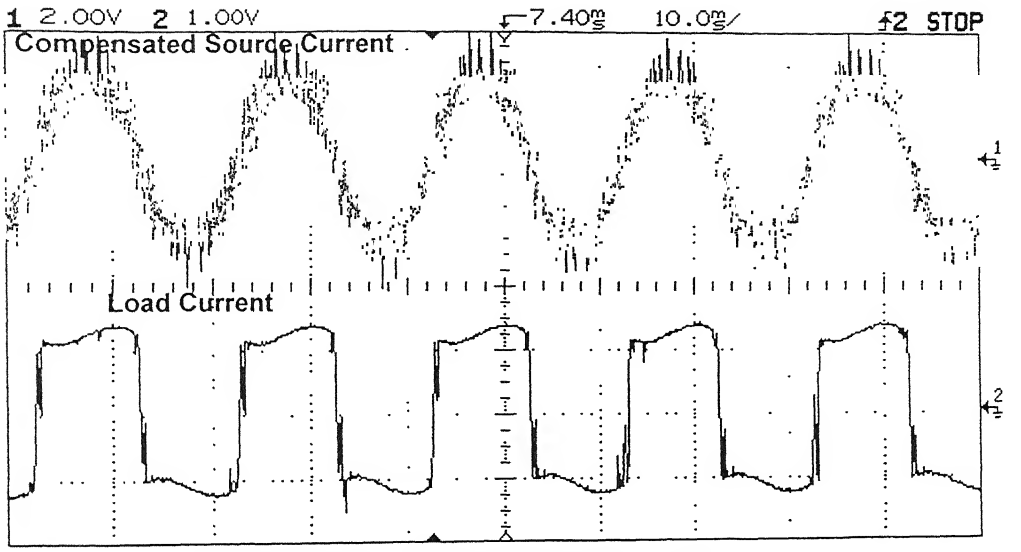


Fig. 7.32 Compensated source current and load current with PWM inverter based AHCC at switching frequency 4.2 kHz.

7.5.1 Losses in PWM inverter based AHCC

The power drawn from the source at different values of dc capacitor voltages with this AHCC are tabulated in Table 7.4. The power drawn from source at the same level of dc capacitor voltages for an RDCLI based AHCC are also tabulated in the same table for comparison purpose. These figures are also presented graphically in Fig. 7.33. As discussed earlier, this power include the load power (i.e., power drawn by the diode-bridge) and the losses in the AHCC. Since the load power is constant for a specific load current, these figures would indirectly reflect the increase in the losses in the AHCC. It is clear that the losses increase with a hard-switched inverter based AHCC.

Table. 7.4 Power drawn from source at different dc capacitor voltages with RDCLI based AHCC and PWM inverter based AHCC.

$V_{dc}(V)$	Power drawn from source (W)	
	RDCLI based AHCC	PWM inverter based AHCC
65	65	80
67	67	82
69	69	85
72	73	88
75	75	92

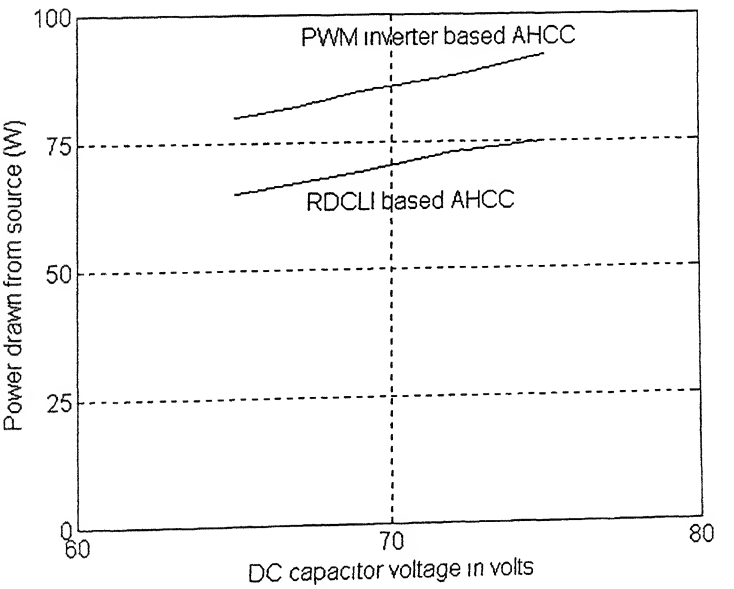


Fig. 7.33 Power drawn from source at different dc capacitor voltage levels with RDCLI based AHCC and PWM inverter based AHCC.

7.6 CONCLUSIONS

The experimental results obtained from the lab prototypes are presented. The proposed current initialization scheme for RDCLI based on state transition equation is experimentally verified. It is shown that that this initial current prediction is quite accurate which in turn ensures the zero crossing of the link voltage at a prescribed time

instant. Zero crossing is achieved at different load conditions. The proposed method is elegant and quite precise, yet simple to implement.

RDCLI provides a high current regulator bandwidth hence makes it better suited candidate for AHCC application. The performance of RDCLI based AHCC in conjunction with PD controller reveals that this compensator is able to compensate load harmonics. This AHCC has a fast transient response. The loss evaluation shows that this compensator is more efficient and would have a high efficiency.

The PWM inverter based AHCC gives a good performance when the inverter switching frequency is high. However, the losses in this AHCC are high compared to its soft-switched counterpart.

The proposed PD controller extracts compensator references accurately, has a fast transient response too. Furthermore its inclusion reduces system losses compared to the inclusion of a PI controller and it has a much faster settling time.

CHAPTER 8

CONCLUSIONS

The general conclusions drawn from this thesis and some suggested new directions are presented in this chapter. The objective of this thesis is to determine a best-suited topology for the power circuit of an active harmonic current compensator and its associated control strategy. The compensator must provide a high current regulator bandwidth, should have a fast transient response and should be efficient.

8.1 GENERAL CONCLUSIONS

The work done in this thesis to achieve the above-mentioned objectives is summarized below.

1. Hard or Soft-switched inverter: The heart of an active harmonic current compensator is a VSI that operates in the current control mode to inject currents into the ac system to cancel out harmonics. The VSI is connected to the ac system through an interface inductor. The current through this inductor is the compensator current. Usually this current is controlled around a reference current in a hysteresis current control mode. If the compensator is able to track its reference current, which is usually non-linear and fast varying in nature accurately, then there is minimum error and ripple in the compensator current. However, this is possible provided the inverter switching frequency is high. The other parameters that affect the compensator current tracking are interface inductor and the driving voltage available across the inductor. These two parameters determine the maximum di/dt that can be achieved by the compensator. For AHCC applications high values of di/dt are necessary to cancel out harmonics as a large inductor would limit the ability of the compensator to cancel harmonic components. A higher value of the dc capacitor

voltage will provide a high driving voltage across inductor but this will increase ripple in the compensator current. For a hard-switched inverter, the increase in frequency will result in increased losses and higher device stresses.

In a soft-switched inverter, the switchings are done when the voltage across the switches is zero. Theoretically therefore there is no switching loss. A resonant dc link inverter can be operated at a high frequency that is 5 to 10 times higher than that of a hard-switched PWM inverter. Therefore an AHCC based on soft-switched inverter will provide a much larger current regulator bandwidth and will have lower losses.

2. Three-Phase or Single-Phase Inverter: It has been shown in this thesis that an AHCC can be realized using a three-phase inverter only if its dc side capacitor is split into half and its neutral point is connected to the neutral point of the load. If a single dc capacitor drives a three-phase inverter, then the tracking performance of the third phase will degrade even under balanced load condition. This configuration will not work at all when the load is unbalanced.

   We have therefore suggested to realize an AHCC for three-phase system using three single-phase inverters that are driven by a single energy storing capacitor. These three inverters are connected to the ac bus through three isolation transformers.

3. Current Initialization: In this thesis a new current initialization scheme is proposed for a resonant dc link inverter (RDCLI). The method of current initialization is based on the state transition analysis of the system as a boundary value problem (BVP). It is shown that for a given load current, it is possible force the dc link voltage to go to zero at a prescribed time by properly choosing the initial dc link current. This technique makes it possible to operate the resonant dc link inverter without any zero-crossing failure, which is an important issue for a satisfactory operation of such an inverter.

4. Compensator Current Extraction: Two simple methods are proposed for the extraction of active fundamental current of the load current. In the first method, the error in the dc capacitor charge is passed through a controller. The output of this

controller gives the peak value of the desired source current. This quantity is then multiplied by the template of the source voltage. The resultant quantity is the instantaneous value of the desired source current. The reference for the compensator is obtained by subtracting this value from the instantaneous value of load current.

In the second method the average value of the capacitor current over one cycle is subtracted from zero and is then passed through a controller. The result obtained through this controller refers to the loss component of the AHCC. This quantity is added with the peak value of the source current (obtained through power calculation) and is then multiplied by the template of source voltage. The resultant quantity gives the instantaneous value of the desired source current. The reference current for the compensator is obtained by subtracting the desired source current value from the instantaneous value of load current. It is possible to extract the compensator reference using the above two methods. However, the second method is slower compared to the first method.

5. PD or PI controller: For the proposed charge based model two controllers are investigated. The PD controller gives a superior performance compared to the PI controller. The PD controller has a faster response, better stability margins. The AHCC losses decrease with a PD controller to a certain extent.

6. Implementation: PC interface is used for the implementation of the proposed current initialization scheme. The use of a PC makes the system more flexible for conducting experiments. This facilitates zero-voltage switching by taking into account of the actual circuit delays and tolerances.

8.2 SCOPE FOR FUTURE WORK

Some suggested new directions of research in the area of AHCC are suggested in this section. These are

1. A soft-switch inverter topology with neutral point clamping needs to be investigated.

2. A superior current control strategy than hysteresis control may be incorporated.

3. Different design aspects of the soft-switched inverter for the link to be operated at a higher frequency may be studied.

4. The compensator performance needs to be investigated for the Δ connected loads.

CHAPTER 8

CONCLUSIONS

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APPENDIX A

DESIGN OF RESONANT INDUCTOR

The inductors used in the resonant link inverters have to carry large circulating currents at high resonant frequencies. In order to reduce the skin effect and to get good quality factor use of Litz wire is recommended. Since litz wire of large current ratings are not easily available, these has been fabricated in the laboratory according to the following defination.

Litz Wire: If the conductor is broken into many small strands, twisted about 10 turns per feet and each strand insulated from each other, the skin effect is lessened. Such wire is known as litz wire.

For single layered coil inductance L is given by

$$L = \frac{0.0395\, a^2 n^2}{b} k$$

where n = number of turns.

a = radius of the coil in cms.

b = length of the coil in cms.

k = function of (2a/b)

Design of Inductor L:

Former: 11.5 cm dia, 14 cms long, air core

Wire:29 SWG enamelled (100 strands each)

Number of turns: 27

Current Rating: 40 A

Value = 52 μH (measured)

The designed value of the inductor is approximately same. In our design

$a = 5.75$ cm

$b = 13.38$ cm

$n = 27$

$k = 0.729$

Substituting these values we will get almost the same result.

Variation of Q factor with Frequency

Frequency in kHz	Q Factor
5	70
10	90
20	110
50	150
100	80

It may be noted that these values are obtained through LCR meter. In the experimental setup the value of Q is taken to be 60 as Q has changed by the other circuit parameters and connecting wires.

APPENDIX B

DETAILS OF PC INTERFACE CARD

Nudaq Data-Acquisition System
PCI-9118 DG/S
PCI-Bus Advanced Data Acquisition Card

SPECIFICATIONS

1. Analog to Digital Converter

- 12 bit ADC using BB ADS7800
- 16 Channel Single-ended or 8 differential channel
- On chip sample and hold
- Input Range (Bipolar ± 5V, Unipolar 0-10V)
- Data throughput 330 kHz (max)
- Overvoltage Protection 70V peak-to-peak
- Accuracy: 0.01 % of FSR ± 1 LSB
- Input amplifier with gains 0.5, 1, 1.5, 5(Program Control)
- Data Transfer through interrupt, Program Control or DMA

2. Digital to Analog Converter

- 12 bit 2 channel using DAC 2813
- Output Bipolar
- Settling time 4.5μ sec

- Linearity $\pm \frac{1}{2}$ bit LSB (max)
- Output Driving ±5 mA

3. General Specification

- I/O Base address: 15 consecutive double word address location
- Connector: 50-pin D-type connector
- Operating Temperature: 0° C -60° C
- Power Consumption: + 5 V @ 560 mA, +12 V @ 60 mA

A 131067